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Development of True Time Delay Circuits

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Table of Contents

Table of Contents 2
List of Figures 2
Objective 4
I. Initial design of the true time delay circuit and planning 4
1.1. Description of the true time delay circuit 4
1.2 Design and simulation of a true time delay circuit 5
1.3 Layout of the board for the first prototype run 8
1.4 Prototype of the true time delay circuit 8
1.5 Measurement results of the true time delay circuit in the first prototype run 9
1.6 Summary 11
II. Development of Compact and Amplitude Compensated True Time Delay Circuit 12
2.1 Description of Amplitude Compensated TTD 12
2.2 Layout of the True Time Delay Circuits with Amplifiers and Attenuator 15
2.3 Prototype and Testing Results of the True Time Delay Version B 16
2.4 Prototype and Testing Results of the True Time Delay A with amplifiers and attenuator. 18
III. Assembly Guidance and Details 22
3.1 Board layout, components and assembly 22
3.2 Host test board and operational states 29
IV. Publication 32
V. Future Work 32
VI. Appendix 32

List of Figures

Fig. 1 Schematic diagram of a true time delay circuit 5
Fig. 2 Cross-section of the HyperBGA board 5
Fig. 3 HFSS model of the meander line – 2048ps line 6
Fig. 4a Simulated S-parameters of the meander lines using HFSS 6
Fig. 4b Simulated delay of the meander lines 7
Fig. 5 a) Measured return losses of the switch, b) measured isolation, c) measured insertion loss and d) switch prototype 7
Fig. 6 Example of the TTD layout in the first prototype run 8
Fig. 7 a) Panel of various test structures, b) delay line with two switches, c) true time delay circuit with bias supply, and d) better view of the true time delay circuit. 9
Fig. 8. Measured and simulated delays of the meander lines 10

Fig. 9. Measured insertion losses of the TTD for 512 ps, 1ns, 2ns, 4ns, and 7.5ns lines with switches 10
Fig. 10. Measured delays of the TTD for 512 ps, 1ns, 2ns, 4ns, and 7.5ns lines with switches 11
Fig. 11. Measured return losses of the TTD for 512 ps, 1ns, 2ns, 4ns, and 7.5ns lines with switches 11
Fig. 12 Circuit diagram of the true time delay circuit with 3 amplifiers, 8 switches, 1 attenuator and 4 amplitude compensation networks 12
Fig. 14 Compensated insertion loss of 512ps, 1024 ps, 2048 ps, and 4096 ps lines 14
Fig. 16 Delays of of 512ps, 1024 ps, 2048 ps, and 4096 ps lines with amplitude compensation circuits 15
Fig. 17: Layout of the true time delay circuit version A (Version A: 29x29mm) 16
Fig. 18 Top view and side view of the BGA TTD prototype (version B) with switches only 17
Fig. 19 BGA TTD version B mounted on a host board 17
Fig. 21 Measured insertion losses of the true time delay circuit of version B 18
Fig. 22 Measured return losses of the true time delay circuit of version B 18
Fig. 23 Revised amplitude compensation network 19
Fig. 24 a) Measured gain of 512ps delay line of the TTD version A and b) Measured gain of 4096 ps delay line of the TTD version A 19
Fig. 25 Top view and side view of the BGA TTD prototype with 3 amplifiers, 8 switches and 1 attenuator 20
Fig. 26 Measured delay of the true time delay circuit of version A 20
Fig. 28 Measured input return losses of the true time delay circuit of version A 22
Fig. 29 Measured output return losses of the true time delay circuit of version A 22
Fig. 30 Simplified top view of the true time delay circuit version A 23
Fig. 31 Top view of the true time delay circuit version A with all labeled components 24
Fig. 32 Bottom layout of the TTD version A that includes the input and output pins using BGA 25
Fig. 33 Bottom view of the true time delay circuit version A 29

Objective: The objective of this project is to develop a true time delay circuit (TTD) that will have 4 bits including 512 ps, 1024 ps, 2048 ps and 4096 ps to total to 7.68 ns from 0.3 to 3 GHz. The TTD will be implemented in a multi-layer printed circuit board using bare dies or packaged solid-state switches. The bits will be gain and slope equalized to achieve constant gain for all bits and over the frequency range of 0.3 to 3 GHz. All of the delay lines, switches and amplifiers will be implemented and packaged in a multi-layer module that can either be surface mounted as a quad flat no lead package (QFN) or connected to a mother board using ball grid arrays (BGA).

I. Initial design of the true time delay circuit and planning

1.1. Description of the true time delay circuit

Fig. 1 shows the architecture of the true time delay circuit. The series delay line and switch configuration are used for the design of the true time delay circuit. The delay lines are designed and implemented in the Endicott Interconnect package technology known as HyperBGA. HyperBGA is a PTFE-based chip carrier technology that has 9 metal layer interconnects and 8 dielectric layers and allows for chip on board or QFN package surfaced mount on the top layer. The entire BGA TTD module can be packaged and mounted on another host board for phased-array antenna applications. Due to the long time delay of 7.68 ns, the true time delay module can be very large. To minimize the size of the TTD module, we employ meander line configurations and multi-layer structures of the HyperBGA board. Fig. 2 demonstrates the cross-section of the HyperBGA boad. The delayed lines are partitioned in multiple layers. For example, the 4.096 ns line is designed as a stripline in the metal layer 8. The ground planes are layers 7 and 9. The 2.048 ns line is designed as a stripline in the metal layer 6. The ground planes are layers 5 (copper-invar-copper) and 7. The 0.5ns, and 1ns line are designed as a stripline in the same metal layer 4. The ground planes are layers 3 and 5. The combination of plated through hole vias, buried vias and blind vias are used to provide the interconnects for all the delay lines. The surface mount packaged switches, amplifiers and passive components are soldered to the top layer of the module. Ball grid arrays are used at the bottom of the module for connection to a host board in a phased array antenna.

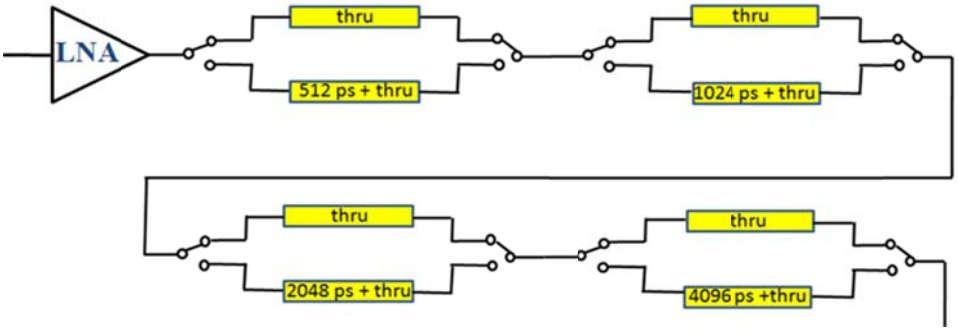


Fig. 1 Schematic diagram of a true time delay circuit

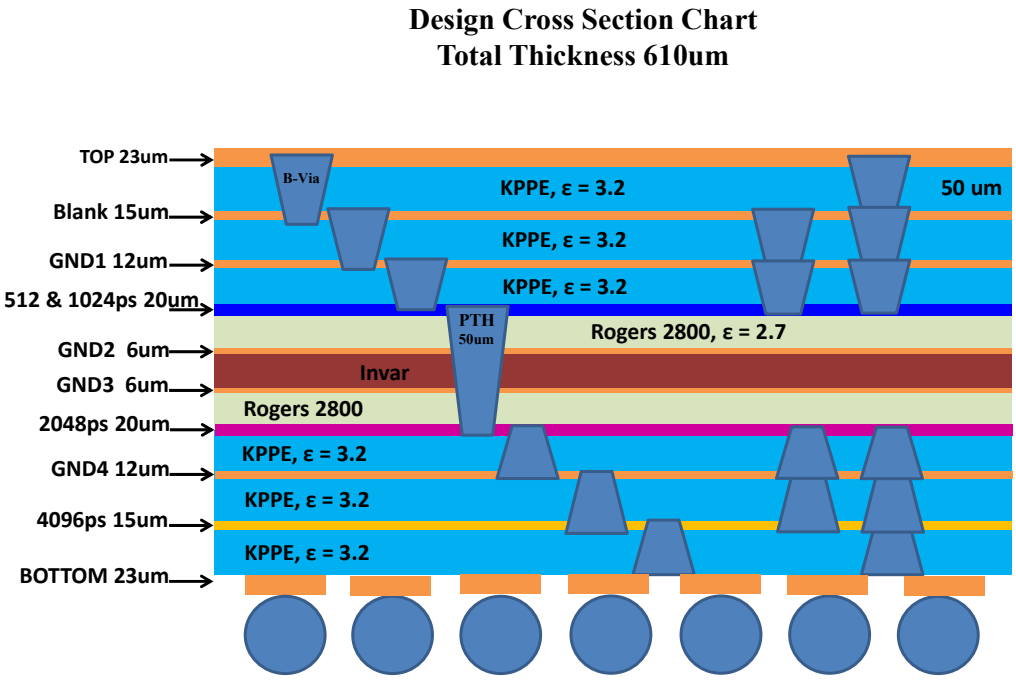


Fig. 2 Cross-section of the HyperBGA board

1.2 Design and simulation of a true time delay circuit

In order to design the delay lines, we first used LINCAL in Agilent Design System (ADS) to determine the nominal width of a 50 Ω stripline or a microstrip line. ADS LINCAL will also provide the effective permittivity of microstrip lines. The delay can be calculated as

$$\tau_d = \frac{l}{v_p}$$

where l is the length of the line and v_p is the approximate phase velocity. For microstrip lines, $v_p = 3\text{x}10^8/\sqrt{\varepsilon_{eff}}$. For striplines, $v_p = 3\text{x}10^8/\sqrt{\varepsilon_r}$. The relative permittivity is between 2.7 and 3.2 given by Endicott Interconnects. We then designed the length and gap of the meander structure to avoid significant coupling and phase changes. We have used full-wave electromagnetic simulation High Frequency Simulation Structure to design and optimize the meander structures. We accounted for parasitics resulted from corners and coupling in the design. The space between the adjacent segments is approximately equal to substrate thickness. The smaller gap between the adjacent meander conductors results in a higher maximum differential phase shift. The length of the segment also is carefully designed to avoid the nonreciprocal effects. In addition, there are a large number of venting holes in the metal layer for processing. We have also accounted for these small holes that cause discontinuity in the ground plane. The S-parameters of the delay line from HFSS were imported to a circuit simulator, ADS. We have also used measured S-parameters of the switches and passive components for the design of the full TTD. The measured S-parameters of the switches were cascaded with the S-parameters of the delay line to design the entire TTD in ADS. Fig. 3 shows an example of the HFSS simulation of the meander line and Fig. 4 shows the simulation results. The simulated return losses of the delay lines are less than 25 dB up to 4 GHz. As the dielectric properties are not very accurate and the venting holes that

could de-tune the return losses, we have laid out several widths in the test board to determine the best return losses. We also anticipate that when the switches are connected to the delay lines, we will have some effects to the overall return losses of the TTD.

The switch is a single pole double throw absorptive switch, part number SKY13286-359LF from Skyworks Solutions. The GaAs pHEMT switch has 55 dB isolation, 0.1-6 GHz bandwidth and an integrated driver all housed in a plastic quad-flat-no-lead package. There are other surface mount switches from Peregrine Semiconductor. We have chosen the Skyworks part due to its high isolation to eliminate any possible resonances. Figures 5 a, b, c and d show the S-parameters of the switch and the prototype board.

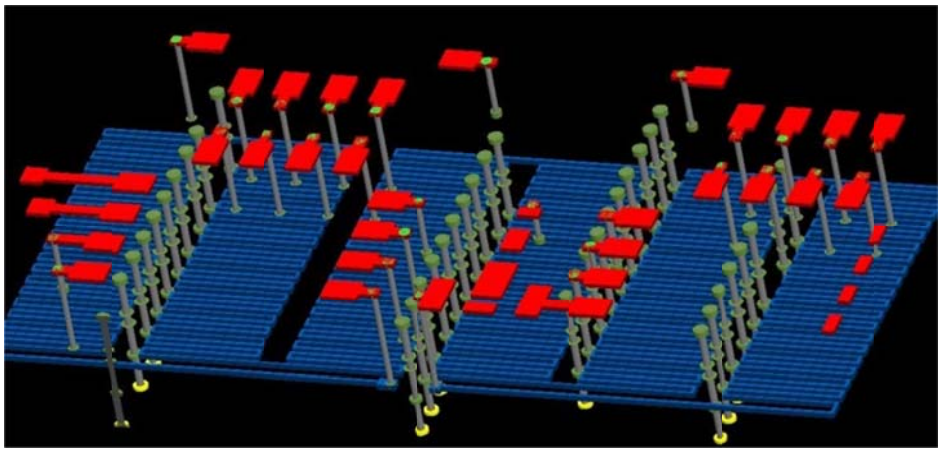


Fig. 3 HFSS model of the meander line – 2048ps line

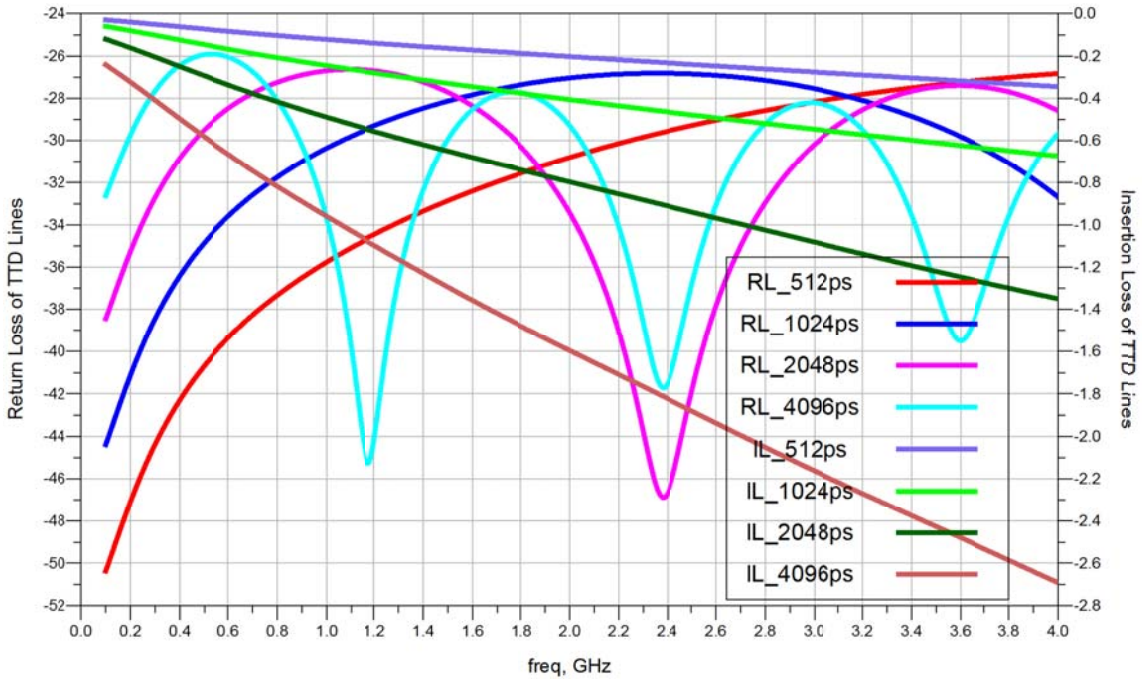


Fig. 4a Simulated S-parameters of the meander lines using HFSS

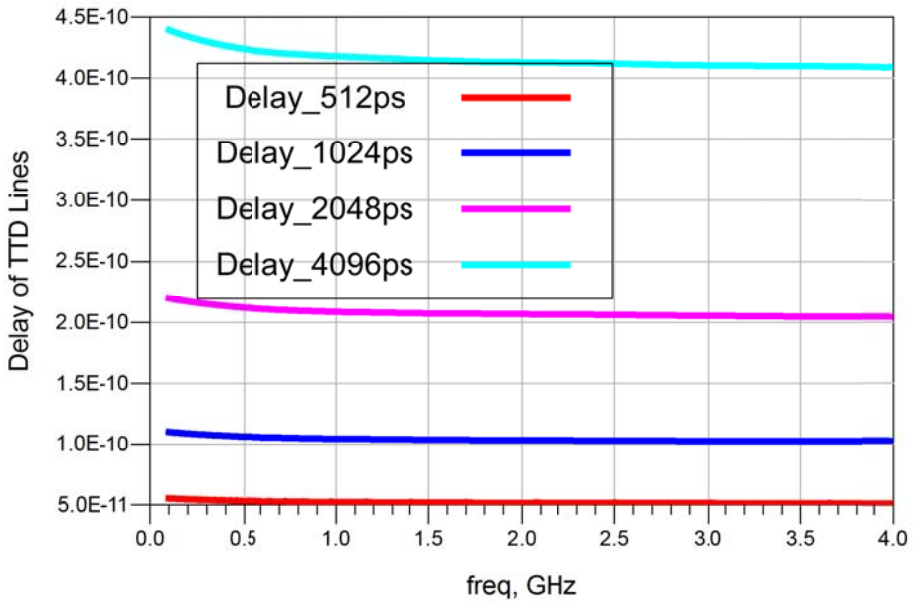


Fig. 4b Simulated delay of the meander lines

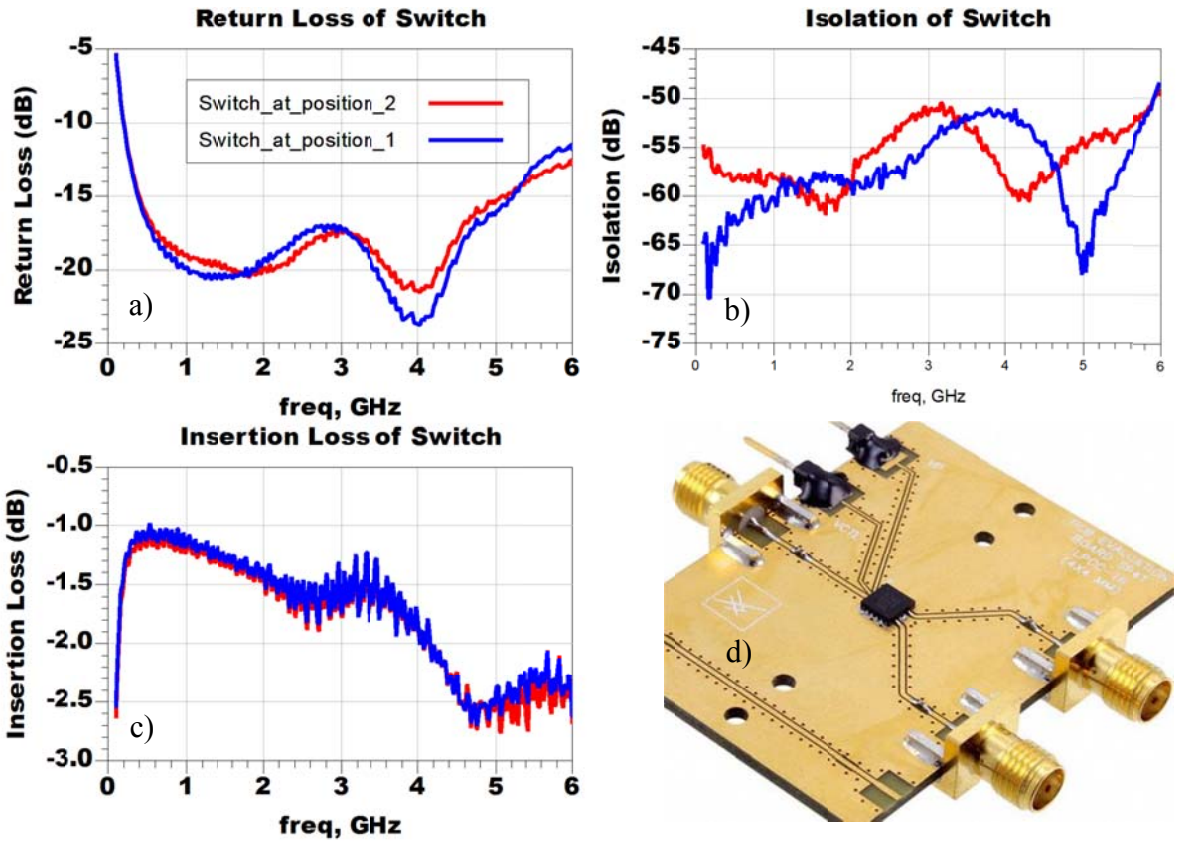


Fig. 5 a) Measured return losses of the switch, b) measured isolation, c) measured insertion loss and d) switch prototype

1.3 Layout of the board for the first prototype run

Based on the design, we have designed and laid out various test structures. They include 512ps lines, 512ps lines with switches, 1ns lines, 1n lines with switches, 2ns lines, 2n lines with switches, 4ns lines, 4ns lines with switches, and a full true time delay circuit. In addition, we have varied the width of the lines to determine the optimal geometry to achieve a good match. We worked with Endicott Interconnects to comply with the design rules and coordinated the fabrication. Once a change was requested from Endicott Interconnects, UC Davis had to fix the layout or re-designed the test structures. The fabrication was performed by Endicott Interconnects. The most time consuming task is to coordinate with Endicott Interconnects to make sure that the design passes design rule check.

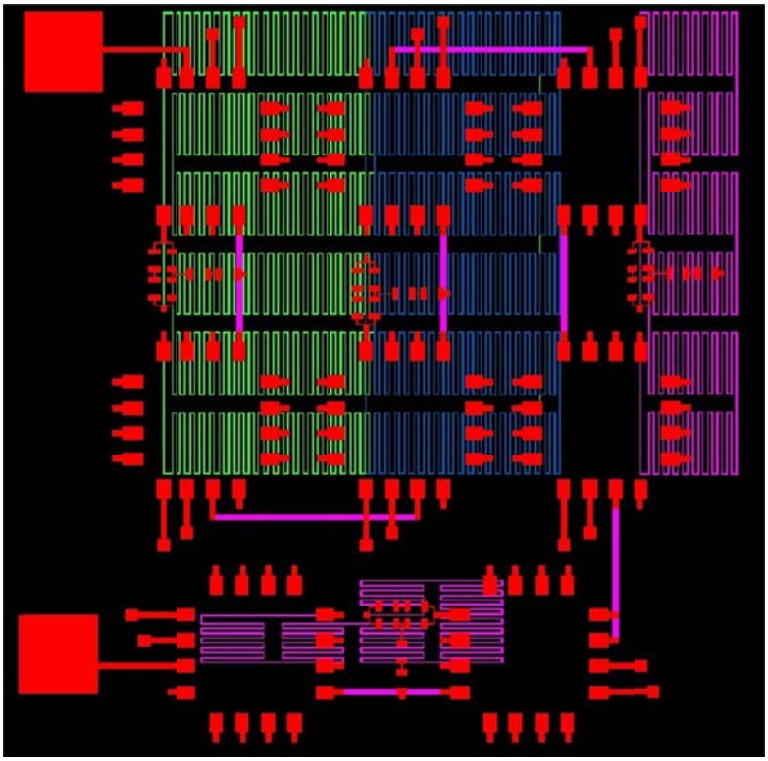


Fig. 6 Example of the TTD layout in the first prototype run

1.4 Prototype of the true time delay circuit

Figure 7 shows several types of fabricated prototypes including 1) an entire panel (Fig. 7a), 2) a delay line with two switches (Fig. 7b), and a full true time delay circuit under test (Fig. 7c and d). The venting holes on the top layer are clearly shown in Fig. 7b. These venting holes in the middle layers present major issues in the design. Both microstrip lines and striplines require a continuous ground for the return current. These venting holes cause discontinuity that would increase inductance and the characteristic impedance of the transmission lines. In addition, the yield of the process is about 50%. We have designed the bias networks and control lines that are interfaced with an FBGA board for testing.

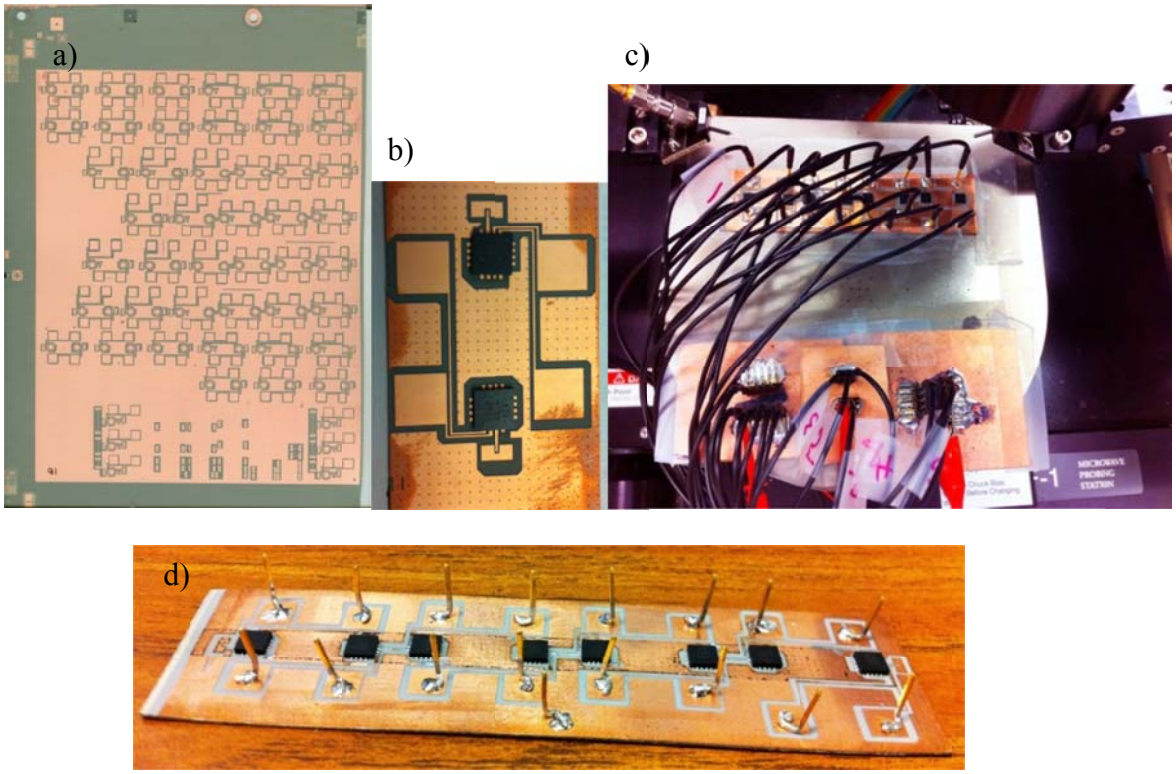


Fig. 7 a) Panel of various test structures, b) delay line with two switches, c) true time delay circuit with bias supply, and d) better view of the true time delay circuit.

1.5 Measurement results of the true time delay circuit in the first prototype run

For each delay lines, we have incorporated a ground signal ground pad for probing. The electrical performance of the delay lines was measured on a Cascade Microtech RF probe station with an Agilent E8364 2-port network analyzer. The probes were calibrated using the standard Thru-Relfect-Line calibration on Picoprobe CS-9 substrate. Using the measured S-parameters, we have extracted the delay of the each line using the following formula:

$$\text{GroupDelay}=-\text{diff}(\text{unwrap}(\text{phaserad}(S21),\pi))/2\pi$$

Fig. 8 demonstrates the comparison of the measured and simulated delay of the meander delay lines. The meander delay lines have a coplanar waveguide probe pads that are used for on-wafer probing to obtain S-parameters. The measurement and simulation results are close. The delay lines are embedded inside the module and are not visible. For the TTD, we have employed an FBGA board (DE1) - from Altera to control the switches. The switches are biased with a voltage of 5V. We first turn on the 512ps delay line and keep other lines in the off positions. We have measured the 512ps delay in the TTD. We then measured the 1ns, 2ns, 4ns lines individually. In addition, we have turned on all the lines and measured the total delay of 7.5 ns. Figs. 9, 10 and 11 demonstrate the measured performance of the TTD module. The return losses of the TTD are less than 10 dB from 0.3 to 6 GHz. The measured S-parameters include the switches and all interconnects. The measured delay of the TTD is close to the design target.

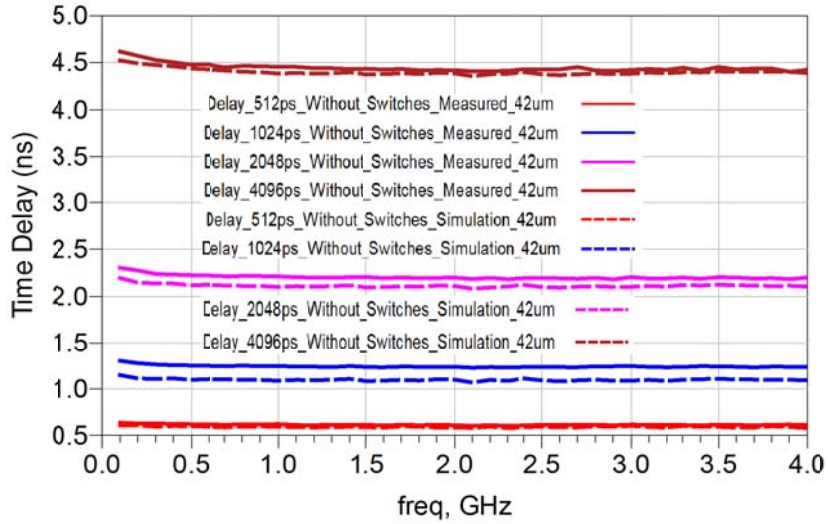


Fig. 8. Measured and simulated delays of the meander lines

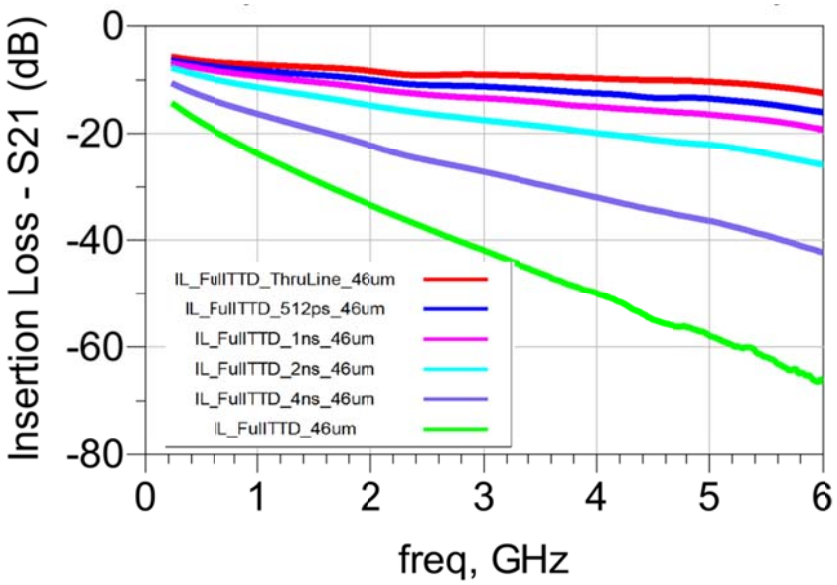


Fig. 9. Measured insertion losses of the TTD for 512 ps, 1ns, 2ns, 4ns, and 7.5ns lines with switches

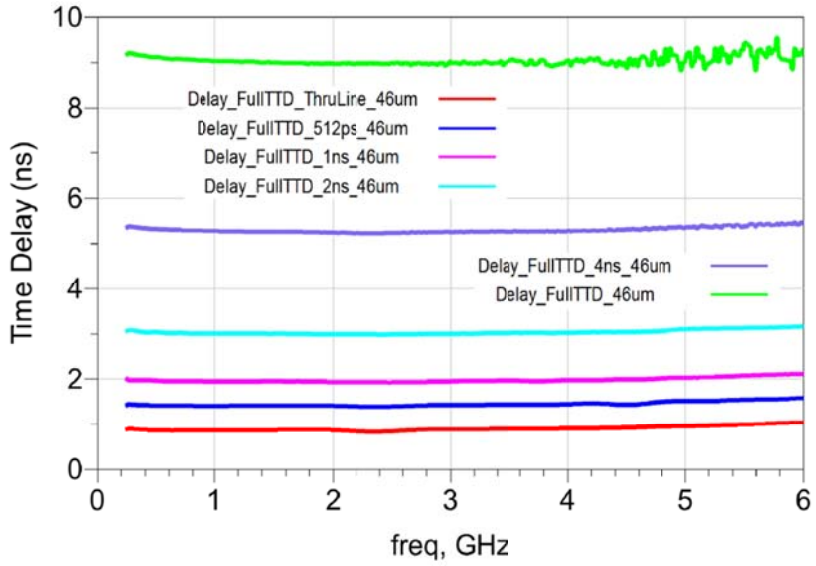


Fig. 10. Measured delays of the TTD for 512 ps, 1ns, 2ns, 4ns, and 7.5ns lines with switches

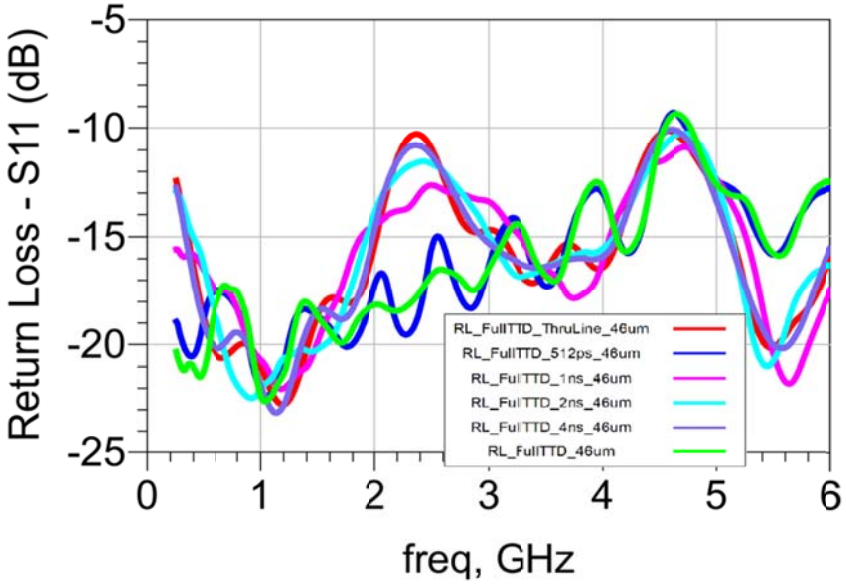


Fig. 11. Measured return losses of the TTD for 512 ps, 1ns, 2ns, 4ns, and 7.5ns lines with switches

1.6 Summary

We have successfully completed the goals of the project in year 1. Our results demonstrate that the simulation and measurements are close and our structures can be used for further design of a true time delay circuit that meets the required specifications.

II. Development of Compact and Amplitude Compensated True Time Delay Circuit

2.1 Description of Amplitude Compensated TTD

We have successfully evaluated the Endicott Interconnects HyperBGA process and developed useful test structures ready for the final design. In the final design, our goal is to provide amplification to reduce the signal losses and to compensate for the amplitude differences with respect to frequency. In addition, we aim to have the entire TTD with amplifiers, attenuators, switches and delay lines in a 1 in by 1 in module. Figure 12 shows the circuit diagram of the entire true time delay circuit.

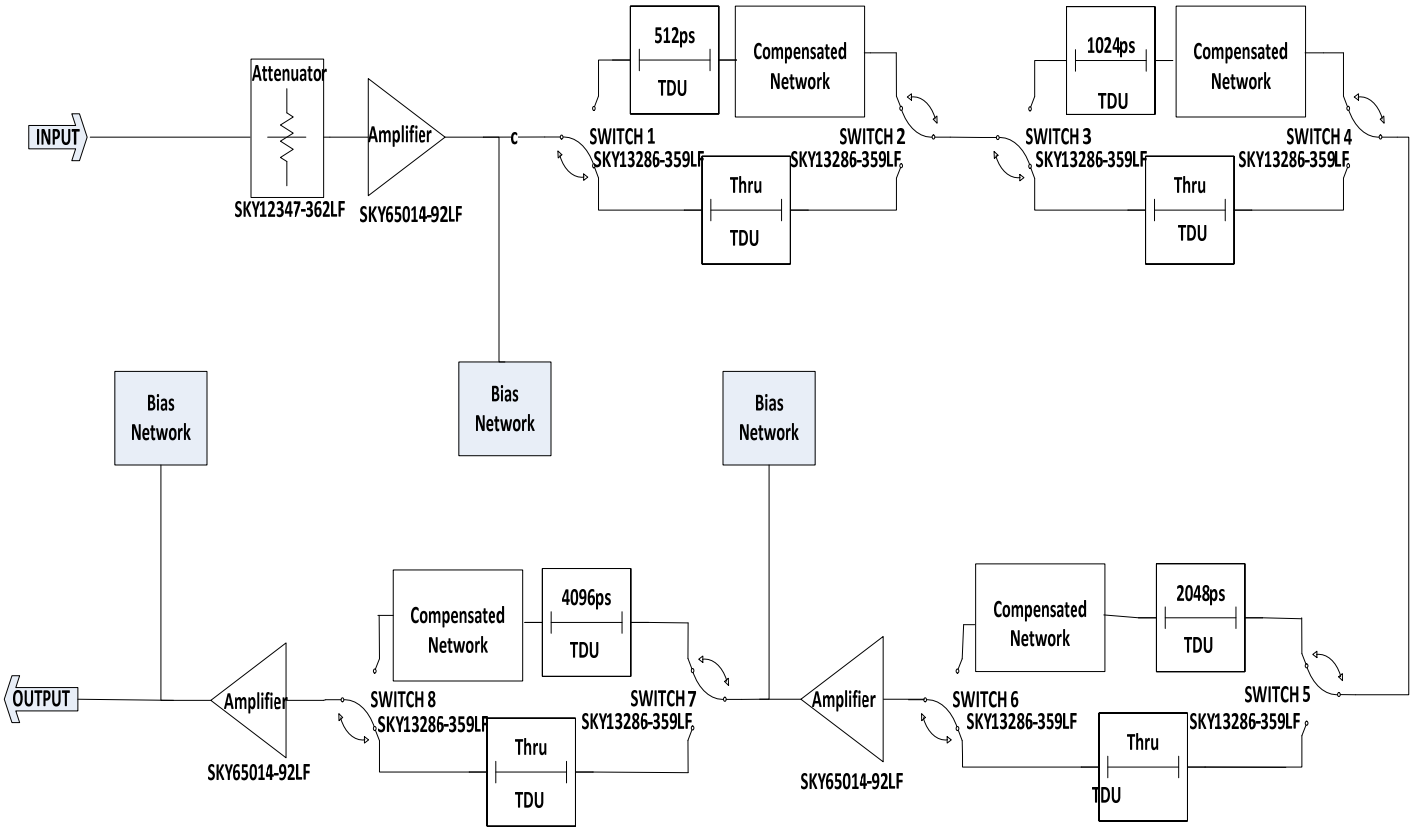


Fig. 12 Circuit diagram of the true time delay circuit with 3 amplifiers, 8 switches, 1 attenuator and 4 amplitude compensation networks

As seen from Fig. 9, the TTD has up to 30dB insertion loss at 3 GHz. The loss increases with respect to frequency. Our goals are 1) to reduce the loss and 2) to compensate the loss so that it is reasonably flat to 3 GHz. To achieve our goals, we have chosen the Skyworks Solutions wide bandwidth amplifiers, part number SKY65015. The amplifier SKY65015 has a small signal gain of 18 dB and an output P_{1dB} of 17 dBm from 0.1 to 6.0 GHz. A total of three amplifiers have been used to bring a total gain to 54 dB to compensate for the losses. We have distributed the amplifiers so that we can deal with the dynamic range of the input signals and avoid saturation or compression at any single stage. In addition, we have used an attenuator from Skywork Solutions, part number SKY12347-362LF. This attenuator has a bandwidth from 0.1 to 3 GHz and a total attenuation of 31.5 dB with 0.5dB least significant bit.

While the gain can boost the signals with respect to frequency, it does not flat the insertion loss with respect to frequency. Therefore, we have developed an amplitude compensation network to flat out the insertion loss. Fig. 13 demonstrates a circuit that provides decreasing losses with respect to frequency to compensate the loss of the 512ps long delay transmission line. The amplitude compensation circuits for 1024 ps, 2048 ps, and 4096 ps delay lines have the same topology with different lumped component values. Table 1 provides the lumped element values for the 512ps, 1024 ps, 2048 ps, and 4096 ps compensation networks. Once the amplitude compensation circuits are designed for each line, we cascade the entire TTD with 3 amplifiers and an attenuator and 8 switches to analyze the entire TTD circuit. Figures 14 and 15 show the simulated return losses and insertion losses of the true time delayed circuit. As seen from Fig. 14, the insertion is within +/- 1 dB up to 3 GHz. The compensated amplitude circuit does not cause any degradation in return losses and delays as seen in Figures 15 and 16.

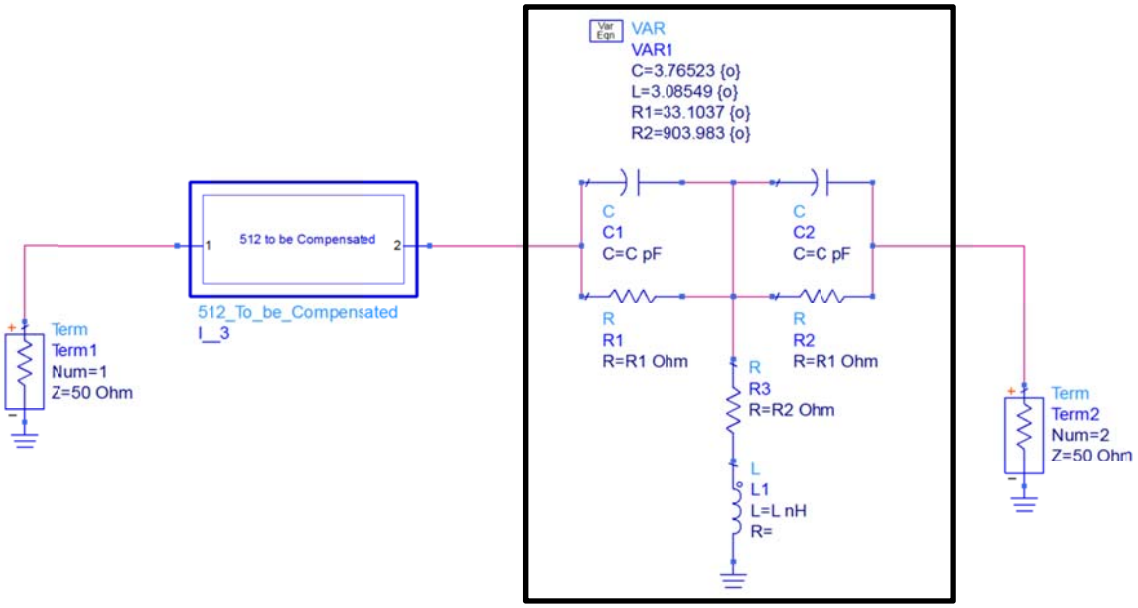


Fig. 13 Amplitude compensation circuit

Table 1. Lumped element values of the compensation circuits

	512 ps	**1024 ps**	**2048 ps**	**4096 ns**
C1 (pF)	3.7	3.9	1.31	0.80
C2 (pF)	3.7	3.9	1.31	0.80
R1 (Ohm)	33.1	30	85.3	138.4
R2 (Ohm)	33.1	30	85.3	138.4
R3 (Ohm)	903.9	993.6	24.2	19.5
L1 (nH)	3.03	1.37	0.62	2.64

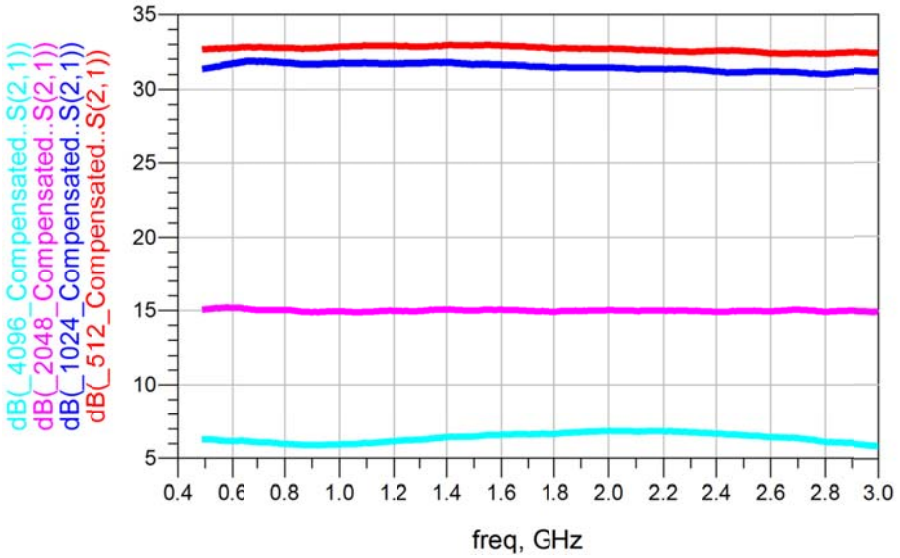


Fig. 14 Compensated insertion loss of 512ps, 1024 ps, 2048 ps, and 4096 ps lines

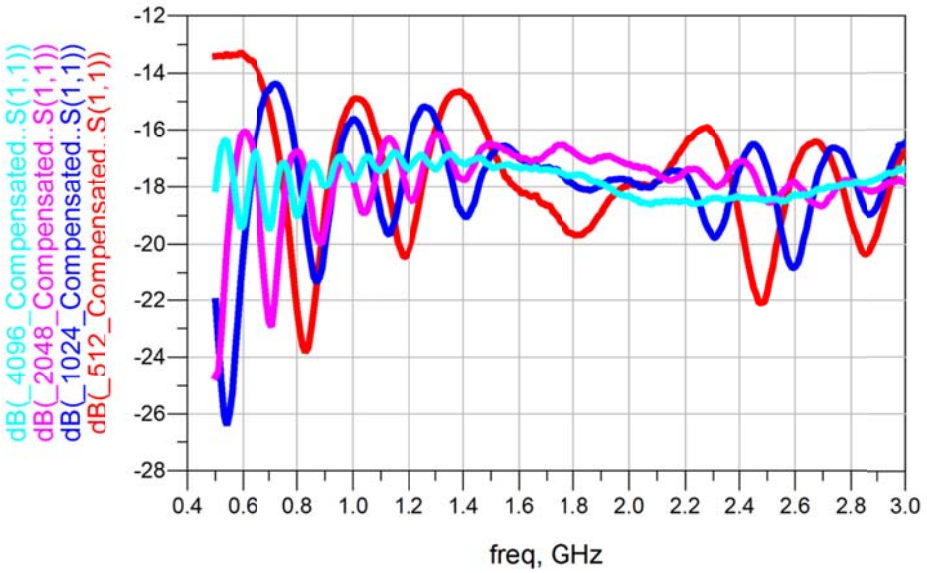


Fig. 15 Return losses of of 512ps, 1024 ps, 2048 ps, and 4096 ps lines with amplitude compensation circuits

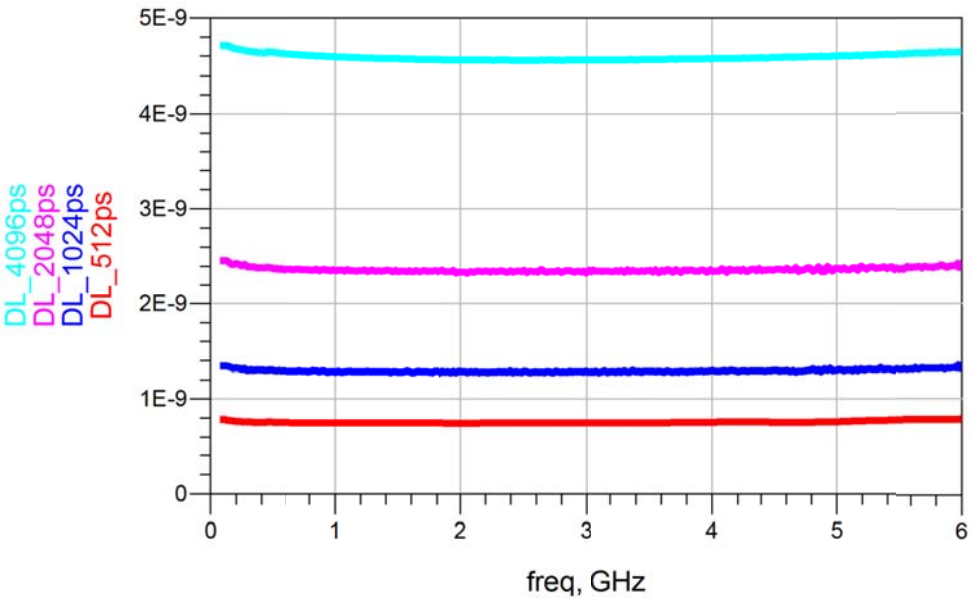


Fig. 16 Delays of of 512ps, 1024 ps, 2048 ps, and 4096 ps lines with amplitude compensation circuits

2.2 Layout of the True Time Delay Circuits with Amplifiers and Attenuator

Based on the design, we have performed the circuit layout using the same cross-section as shown in Fig. 2. In this second board run, we have designed and laid out 4 versions. They are listed in Table 2. Fig. 17 shows an example of the layout of version A with a few layers. Version A is the ultimate circuit that we would like to build for the project. Other versions are back-up and test circuits. Note that the entire layout files have been stored in a server so that AFRL can download. The server is http://bluemoon.ece.ucdavis.edu; **Usernamme**: Name ; **Password:** xyz . Note that Endicott Interconnects went through a difficult period and was acquired and changed to now I3 Electronics. Therefore, we have a long delay on the project. The board was effectively fabricated under I3 Electronics name.

Table 2. Versions of the layout

Version	**Description**	**Size**
A	True time delay circuit, 3 amplifiers, 1 attenuator, 8 switches, and 4 amplitude compensation networks with BGA interconnects	29 mm x 29 mm
A1	True time delay circuit, 3 amplifiers, 1 attenuator, 8 switches, and 4 amplitude compensation networks without BGA interconnects for debugging purposes	40 mm x 40 mm
B	True time delay circuit and 8 switches with BGA interconnects	27 mm x 27 mm
B1	True time delay circuit and 8 switches without BGA interconnects for debugging purposes	27 mm x 27 mm

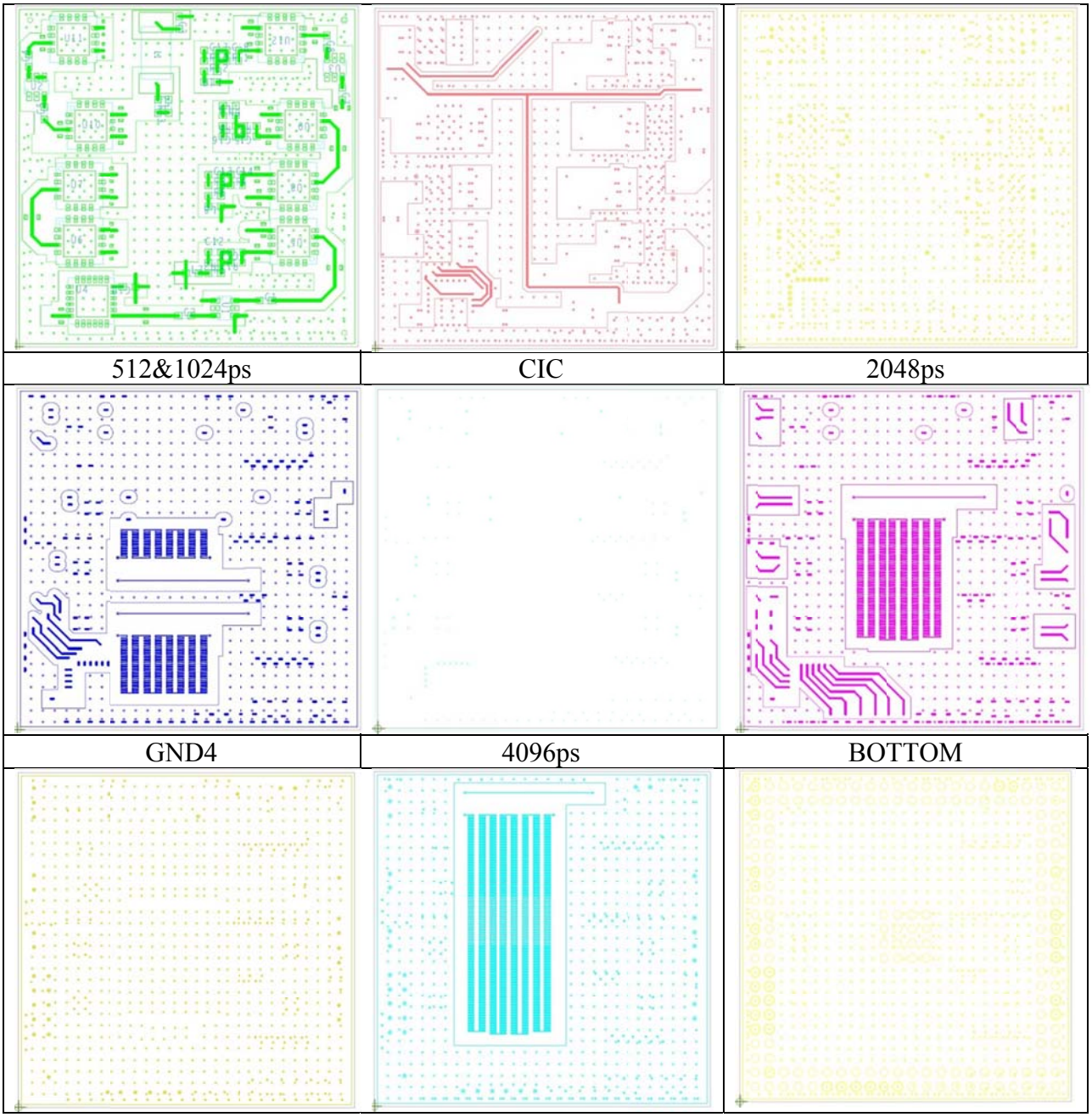


Fig. 17: Layout of the true time delay circuit version A (Version A: 29x29mm)

2.3 Prototype and Testing Results of the True Time Delay Version B

Fig. 18 shows the prototype of the true time delay circuit version B without any amplifiers in the second prototype board run. The solder assembly is performed at UC Davis. Fig. 19 shows the TTD mounted on a host board using BGA. We have conducted measurements using an Agilent Performance Network Analyzer (PNA) with coaxial connectors. We have calibrated the PNA to the coaxial ends and measured the TTD through a host board that provides DC power supply connections. Fig. 20 shows the measured delay of the TTD version B while

Figures 21 and 22 show the measured insertion losses and return losses from the TTD version B. Note that the host board causes some additional losses and ripple at high frequency near 3 GHz.

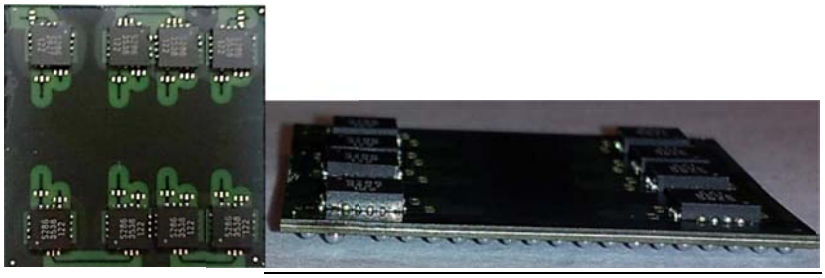


Fig. 18 Top view and side view of the BGA TTD prototype (version B) with switches only

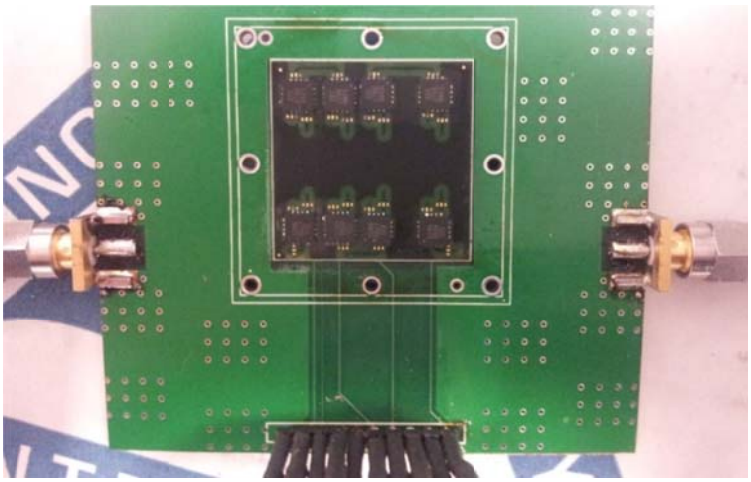


Fig. 19 BGA TTD version B mounted on a host board

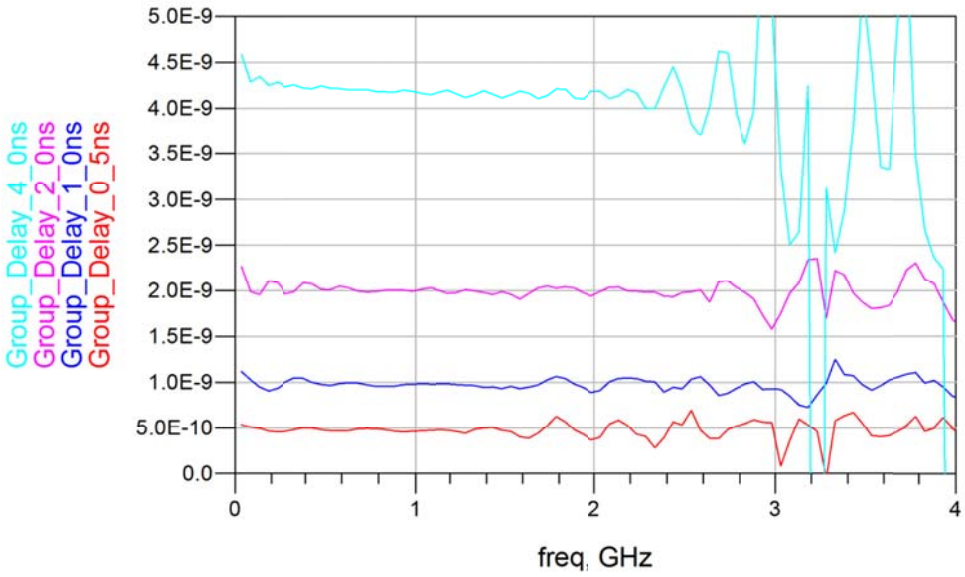


Fig. 20 Measured delay of the true time delay circuit of version B

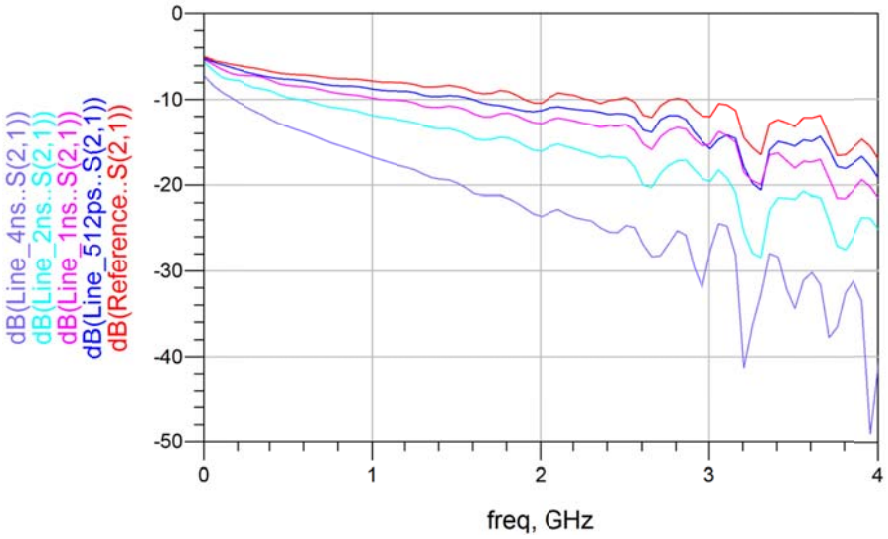


Fig. 21 Measured insertion losses of the true time delay circuit of version B

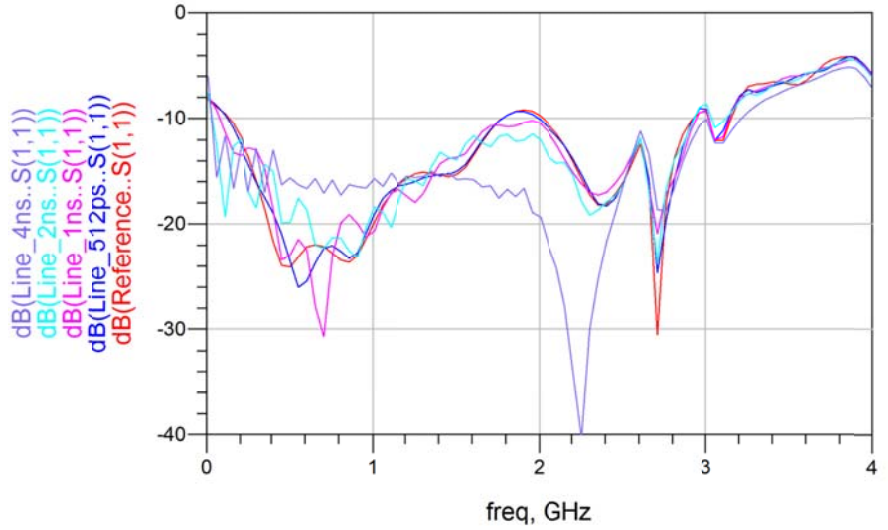


Fig. 22 Measured return losses of the true time delay circuit of version B

Summary: We have successfully developed the true time delay circuit that can provide proposed delay.

2.4 Prototype and Testing Results of the True Time Delay A with amplifiers and attenuator

We ran into a few issues with the final prototype. We had low frequency oscillation from the amplifier and the amplitude compensation networks did not perform due to non-ideal components on the actual board. We have re-designed and re-tuned the amplitude compensation circuits for the final prototype. Fig. 23 shows the revised amplitude compensation network. The new compensation network contains an additional capacitor in parallel with the shunt inductor. The value of the additional capacitor was selected for which the LC tank will resonate right above the top frequency range to compensate for the loss at high frequency. Fig. 24 shows the

measured gain for the 512ps and 4048ps delay lines. The gain flatness is about +/- 2 dB. If tight tolerant passive components are available, the flatness can be reduced to +/- 1dB. The amplitude compensation networks for 1024 ps, 2048 ps and 4096 ps lines have the same topology. Table 3 shows the values of lumped components for the revised amplitude compensation networks.

Table 3. Lumped element values of the revised amplitude compensation circuits

	512 ps	**1024 ps**	**2048 ps**	**4096 ns**
C31 (pF)	3	4	5	4
C32 (pF)	3	4	5	4
C33 (pF)	1.5	1	1	1
R4 (Ohm)	33	25	18	8
R5 (Ohm)	33	33	33	33
R6 (Ohm)	33	33	33	33
L15 (nH)	1.5	1.5	1.5	1.5

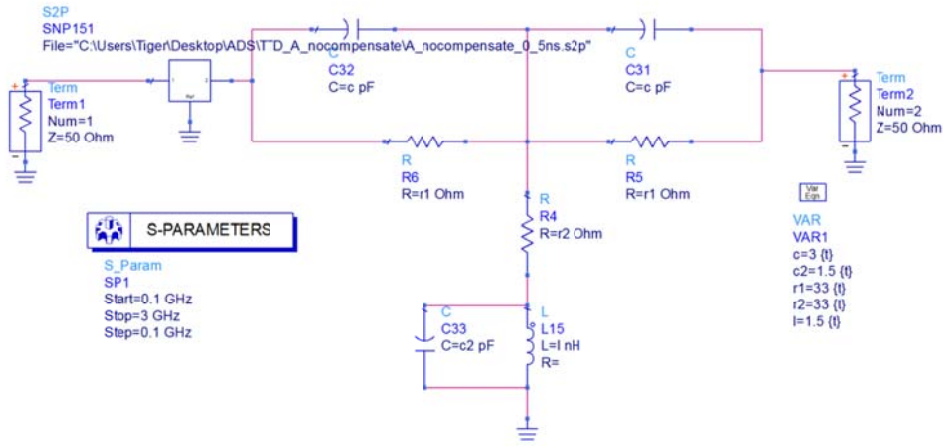
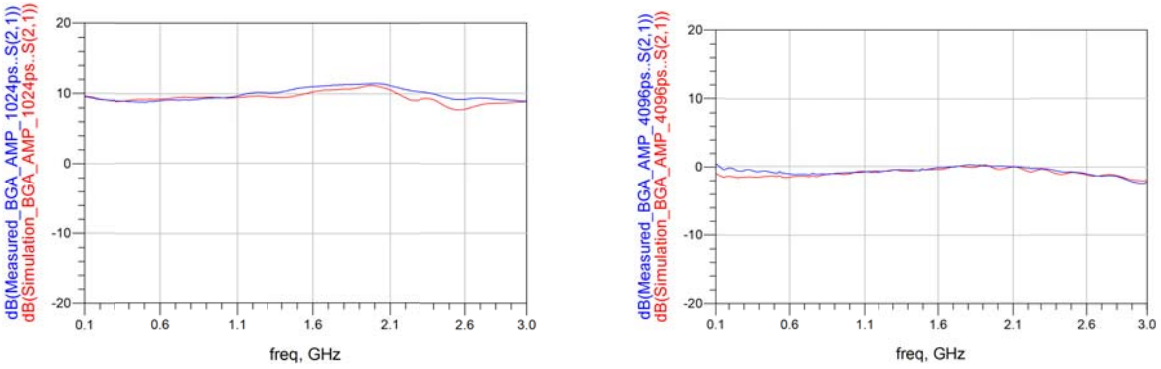


Fig. 23 Revised amplitude compensation network



a) b)

Fig. 24 a) Measured gain of 512ps delay line of the TTD version A and b) Measured gain of 4096 ps delay line of the TTD version A

Fig. 25 shows the prototype of the true time delay circuit version A with 3 amplifiers, 8 switches, 1 attenuator and 4 passive amplitude compensation networks. The prototype is mounted on a host board using BGA. We have to re-work the TTD module to add the additional capacitors for the amplifiers to remove low frequency oscillation that causes ripples in the delay. Fig. 26 shows the measured delay of the TTD module version A that includes 3 amplifiers, 8 switches, 1 attenuator and 4 amplitude compensation circuits for each delay line. The delay is fairly constant with respect to frequency. Fig. 26 shows the measured gain of of the TTD module that includes 3 amplifiers, 8 switches, 1 attenuator and amplitude compensation circuits for each delay line. The gain flatness is within +/- 2dB with respect to frequency. Fig. 27 shows the measured input return loss of the TTD module. The return loss is below -10 dB up to 3 GHz. Fig. 28 shows the measured output return loss of the TTD module.

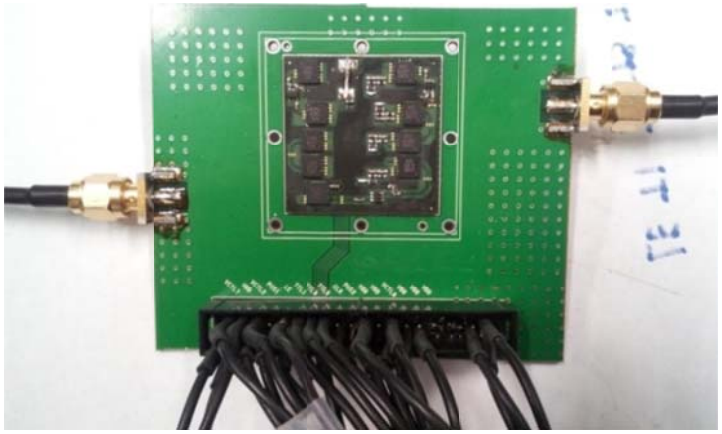


Fig. 25 Top view and side view of the BGA TTD prototype with 3 amplifiers, 8 switches and 1 attenuator

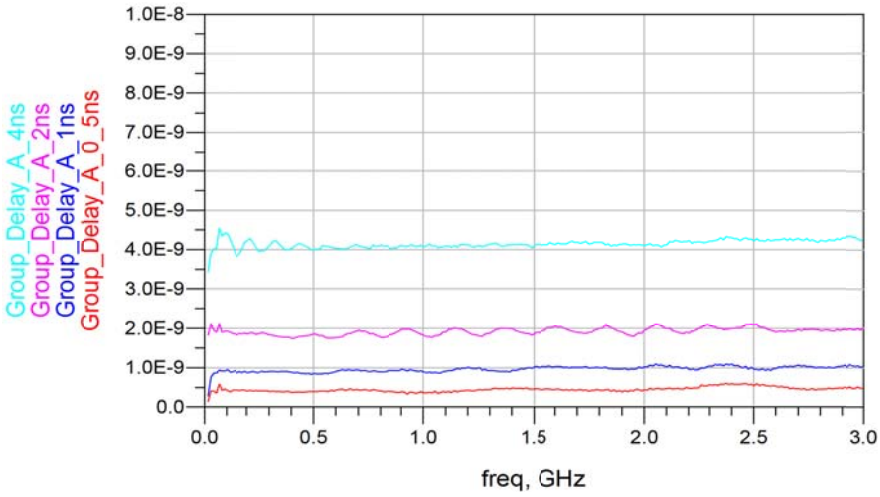
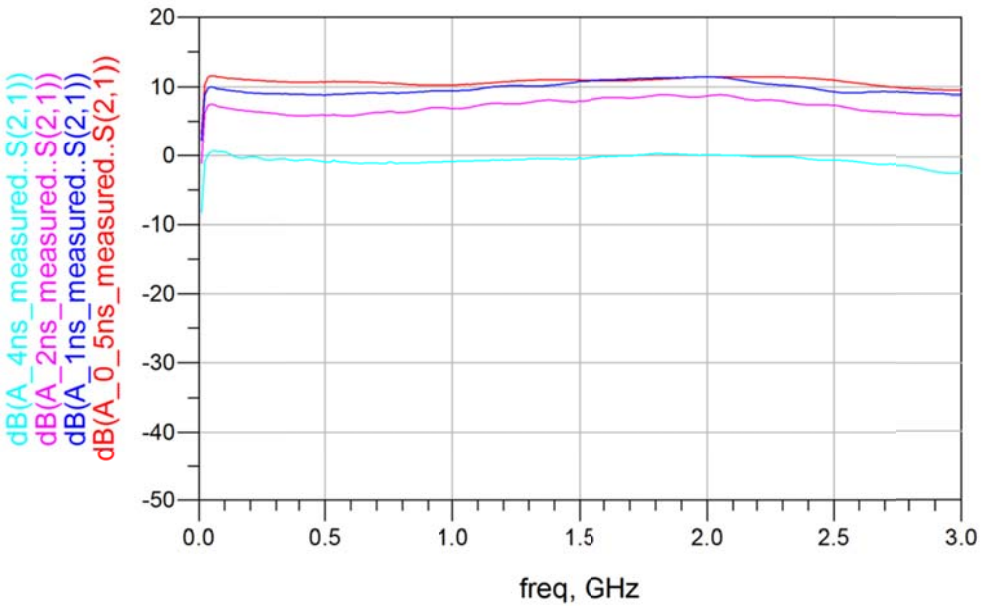
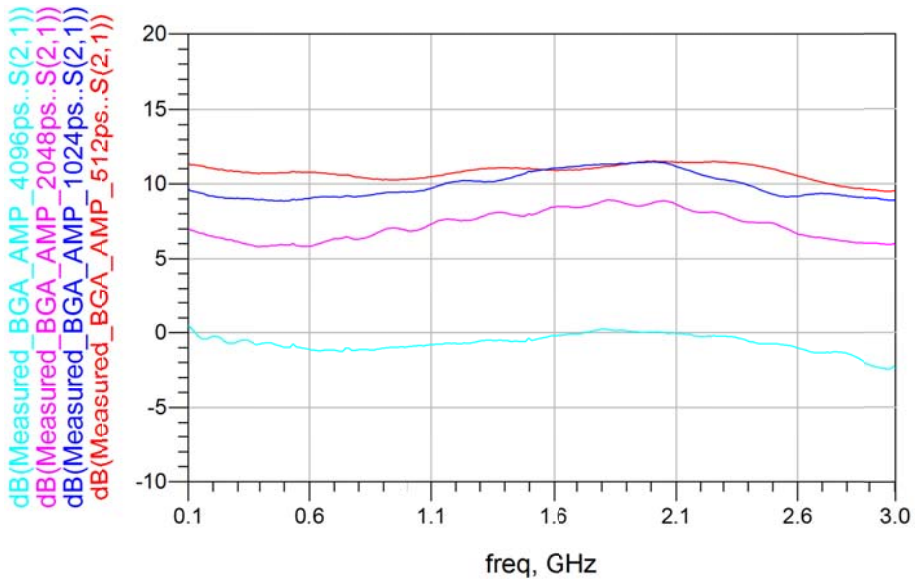


Fig. 26 Measured delay of the true time delay circuit of version A



a)



b)

Fig. 27 a) Measured gain of the true time delay circuit of version A and b) Measured gain of the true time delay circuit of version A in a smaller scale

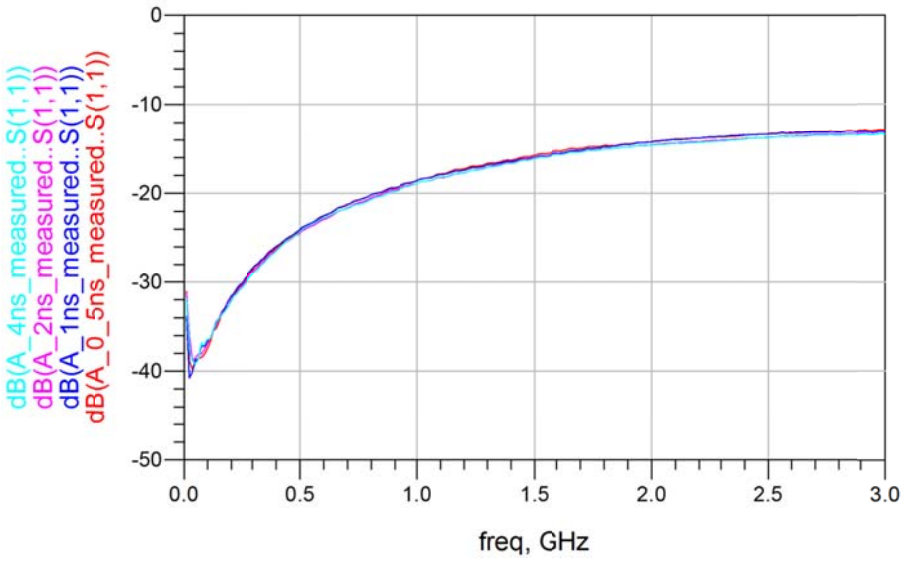


Fig. 28 Measured input return losses of the true time delay circuit of version A

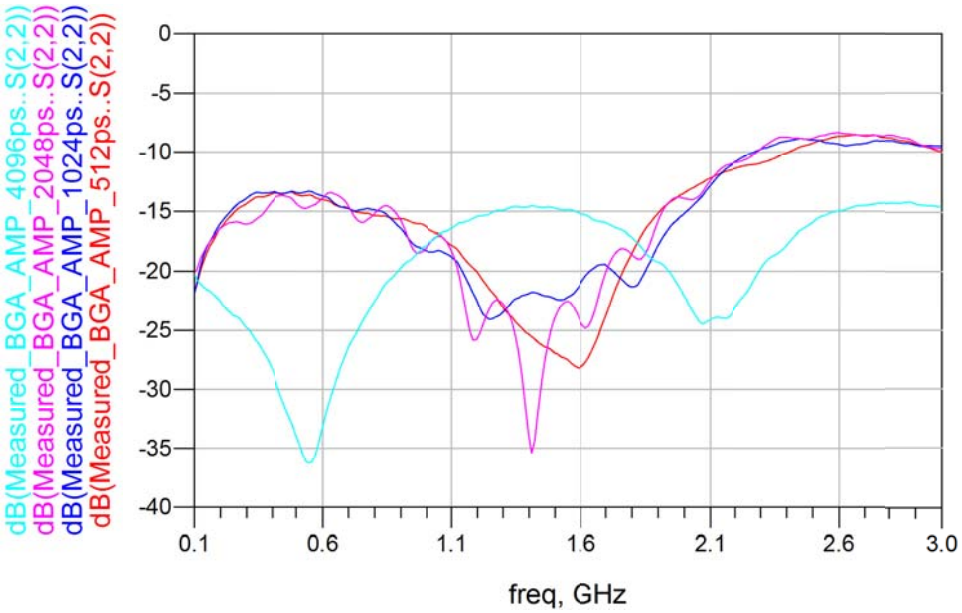


Fig. 29 Measured output return losses of the true time delay circuit of version A

Summary: We have successfully designed and developed a true time delay circuit that meet our proposed goals.

III. Assembly Guidance and Details

3.1 Board layout, components and assembly

Fig. 30 shows the simplied top view of the TTD module version A. Fig. 31 shows the detailed schematic diagram of the TTD module version A with all components placed on the layout. Fig. 32 shows the TTD version A bottom layout that has the input and output pins using BGA connections. The definition of each of the input and output BGA pins in Fig. 32 is listed

in Table 4. Table 5 lists the bill of materials of components indicated in the layout Fig. 30 and 31. Tables 6 and 7 show the operational states for the 8 switches and 1 attenuator.

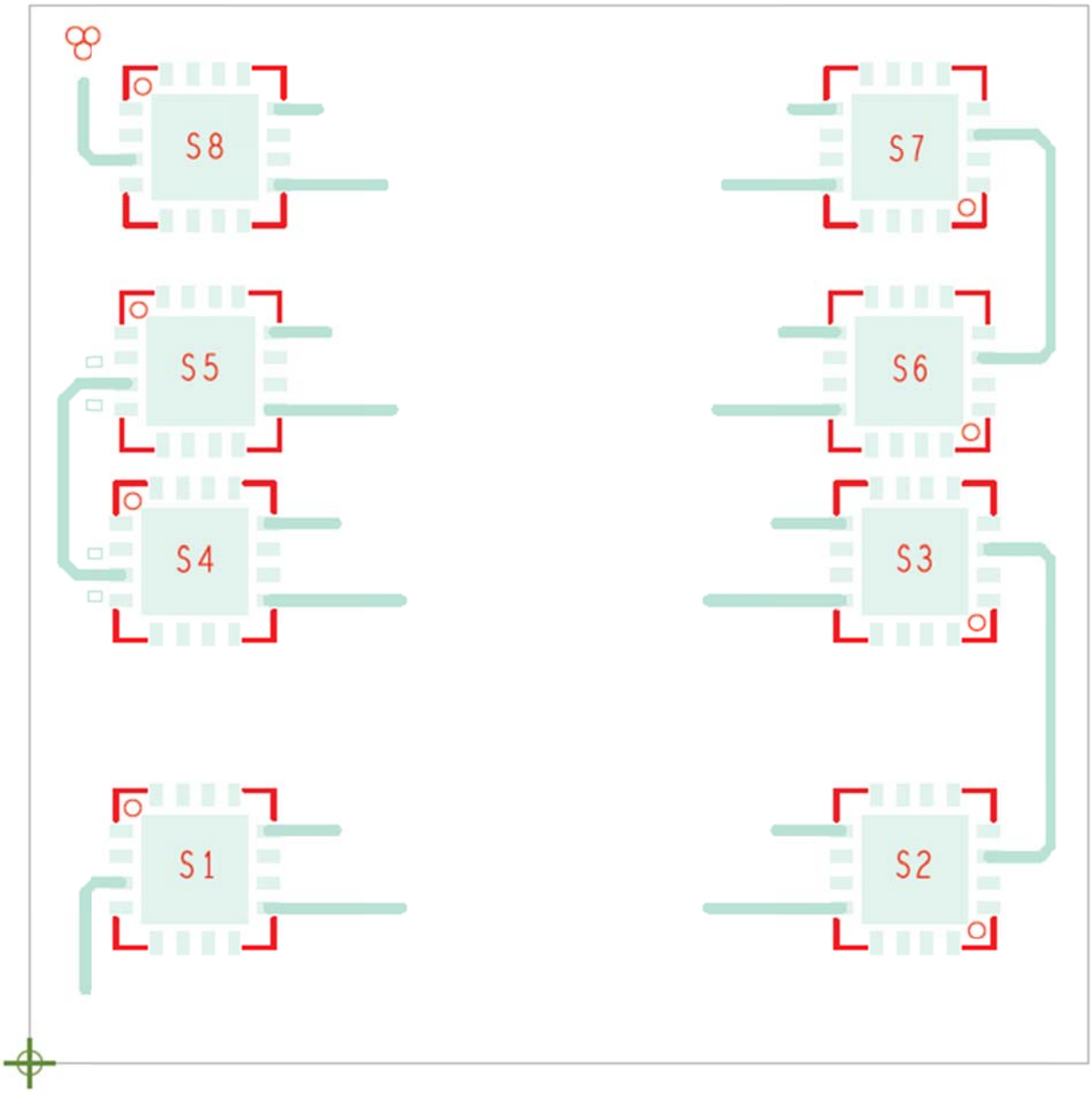


Fig. 30 Simplified top view of the true time delay circuit version A

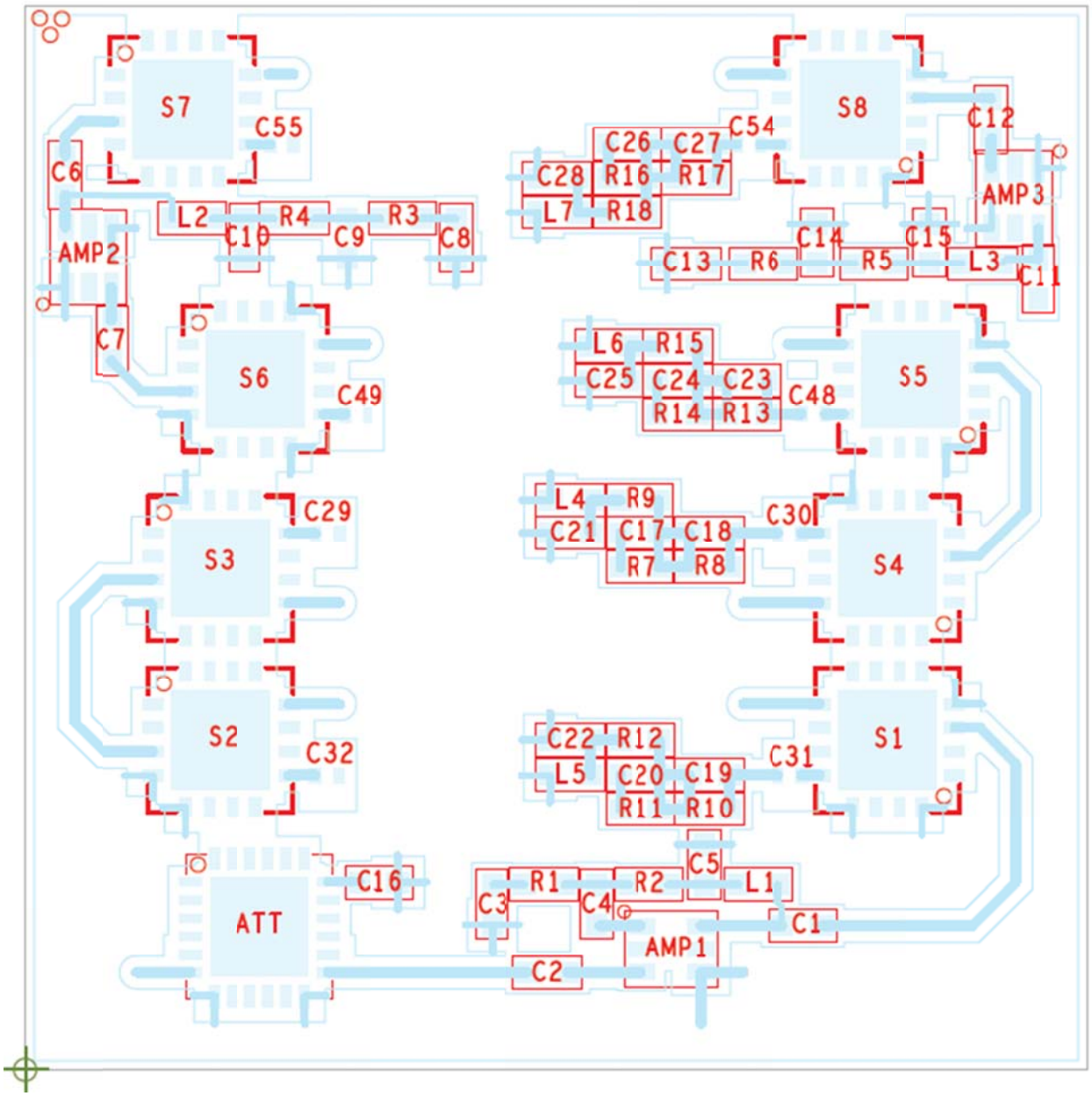


Fig. 31 Top view of the true time delay circuit version A with all labeled components

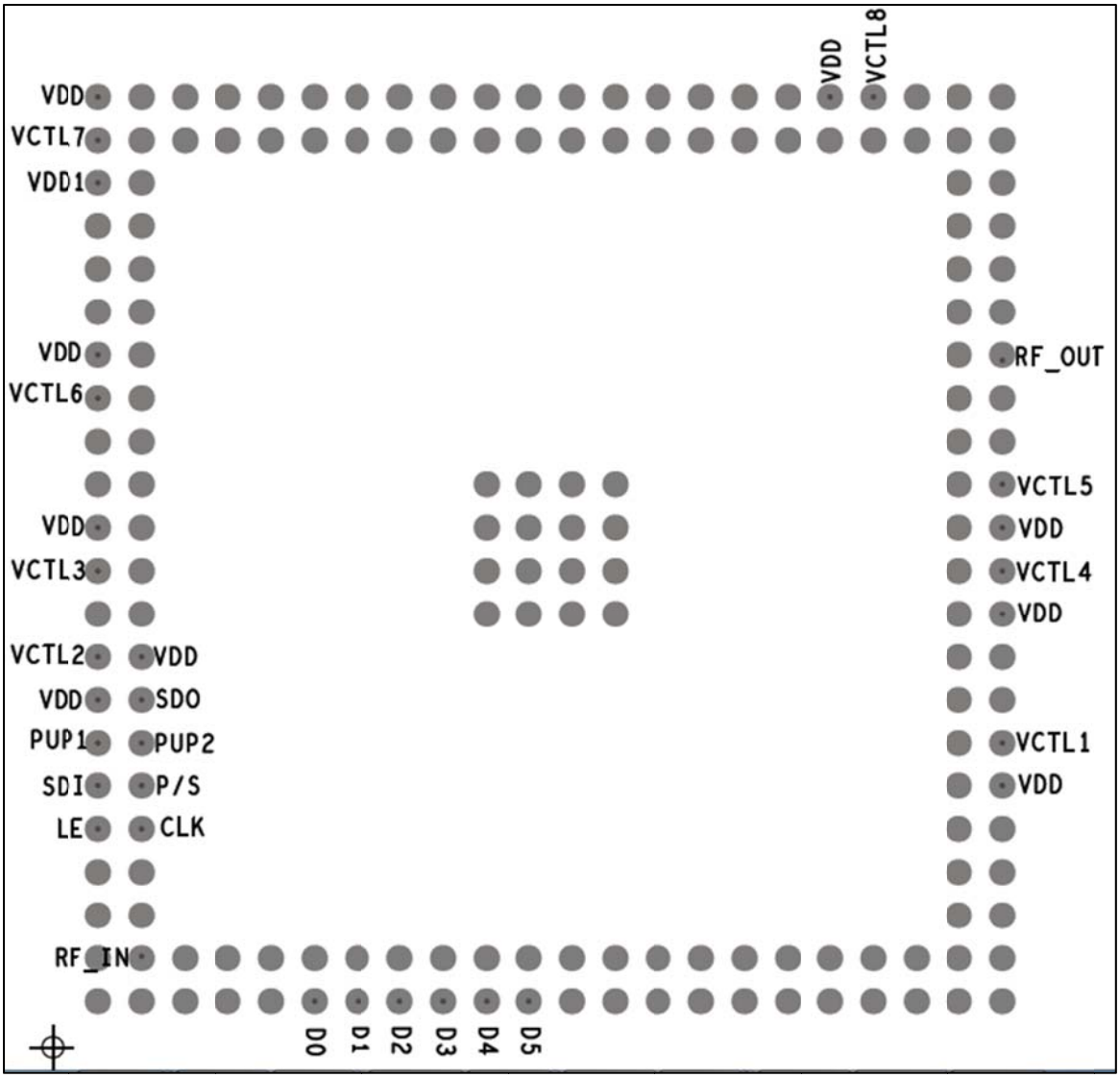


Fig. 32 Bottom layout of the TTD version A that includes the input and output pins using BGA

Table 4. List of input and output BGA pins of the bottom layout TTD Version A of Fig. 32

Pin #*	Name	Description	Pin #	Name	Description
442	RF_IN	RF TTD Input	288	VDD	DC power supply = 5V
468	D0	TTL/CMOS DC control pin for parallel mode operation. D0 is LSB.	243	VCTL3	DC switch control pin for switch #3. Switches insertion loss state from RFC to J1 or J2 (see Table).
469	D1	TTL/CMOS DC control pin for parallel mode operation	221	VDD	DC power supply = 5V
470	D2	TTL/CMOS DC control pin for parallel mode operation	155	VCTL6	DC switch control pin for switch #6. Switches insertion loss state from RFC to J1 or J2 (see Table).
471	D3	TTL/CMOS DC control pin for parallel mode operation	133	VDD	DC power supply = 5V
472	D4	TTL/CMOS DC control pin for parallel mode operation	45	VDD1	DC power supply for amplifiers. Supply current = 210 mA
473	D5	TTL/CMOS DC control pin for parallel mode operation. D5 is MSB.	23	VCTL7	DC switch control pin for switch #7. Switches insertion loss state from RFC to J1 or J2 (see Table).
375	LE	On rising edge of pulse, shifts six most recent clocked-in bits to set attenuation state. In parallel mode, if latch enable is logic high, changes to pins 19 to 24 occur directly. If latch enable is logic low, the attenuator does not change states until the signal is raised.	1	VDD	DC power supply = 5V
376	CLK	Serial clock input	18	VDD	DC power supply = 5V
353	SDI	Serial data input	19	VCTL8	DC switch control pin for switch #8. Switches insertion loss state from RFC to J1 or J2 (see Table 6).

354	P/S	Selects serial or parallel operation. Logic low enables parallel mode.	154	RF_OUT	RF TTD Output
331	PUP1	Sets device power-up attenuation state.	220	VCTL5	DC switch control pin for switch #5. Switches insertion loss state from RFC to J1 or J2 (see Table 6).
332	PUP2	Sets device power-up attenuation state.	242	VDD	DC power supply = 5V
309	VDD	DC power supply = 5V	264	VCTL4	DC switch control pin for switch #4. Switches insertion loss state from RFC to J1 or J2 (see Table 6).
310	SDO	Serial data output	286	VDD	DC power supply = 5V
287	VCTL2	DC switch control pin for switch #2. Switches insertion loss state from RFC to J1 or J2 (see Table 6).	352	VCTL1	DC switch control pin for switch #1. Switches insertion loss state from RFC to J1 or J2 (see Table 6).
374	VDD	DC power supply = 5V	Other	GND	Ground

*Pin # is the identification of the real layout in Allegro file stored in the bluemoon server.

Table 5. Bill of materials for the TTD Version A

#	Qty	Name*	Manufacturer	Description	Part Number	Digikey Part Number
1	14	C1,C2,C6,C7, C11,C12,C29, C30,C31,C32, C48, C49,C54,C55	Taiyo Yuden	CAP CER 0.047UF 16V 10% X7R 0201	EMK105B7473KV-F	587-1225-1-ND
2	3	C3,C8,C13	Samsung Electro-Mechanics America, Inc	CAP CER 1UF 6.3V 5% X5R 0402	CL05A105JQ5NNNC	1276-1444-1-ND
3	4	C4,C9,C14,C16	Murata Electronics North America	CAP CER 10000PF 16V 10% X7R 0402	BLM15HD102SN1D	1276-1500-1-ND
4	3	C5,C10,C15	Samsung Electro-Mechanics America, Inc	CAP CER 1000PF 50V 10% X7R 0402	CL05B102KB5NCNC	1276-1492-1-ND
5	4	C17,C18,C26, C27	TDK Corporation	CAP CER 4PF 50V NP0 0402	C1005C0G1H040B050BA	445-4876-1-ND
6	2	C19,C20	TDK Corporation	CAP CER 3PF 50V NP0 0402	C1005C0G1H030B050BA	445-4869-1-ND
7	3	C21,C25,C28	Samsung Electro-Mechanics America, Inc	CAP CER 1PF 50V NP0 0402	CL05C010BB5NNNC	1276-1237-1-ND
8	1	C22	TDK Corporation	CAP CER 1.5PF 50V NP0 0402	C1005C0G1H1R5B050BA	445-4858-1-ND
9	2	C23,C24	Samsung Electro-Mechanics America, Inc	CAP CER 5PF 50V NP0 0402	C1005C0G1H050B050BA	1276-1603-1-ND
10	3	L1,L2,L3	Murata Electronics North America	FILTER CHIP 1000 OHM 250MA 0402	BLM15HD102SN1	490-4003-2-ND
11	4	L4,L5,L6,L7	Murata Electronics North America	INDUCTOR 1.5NH +/-0.1NH 1A	LQW15AN1N5B00D	535-10351-1-ND
12	6	R1,R2,R3,R4, R5,R6	Samsung Electro-Mechanics America, Inc	RES 4.7 OHM 1/16W 5% 0402	RC1005J4R7CS	1276-4320-1-ND
13	9	R7,R8,R10,R11,R12,R13,R14, R16,R17	Samsung Electro-Mechanics America, Inc	RES 33 OHM 1/16W 1% 0402	RC1005F330CS	1276-3912-1-ND
14	1	R9	Samsung Electro-Mechanics America, Inc	RES 24.9 OHM 1/16W 1% 0402	RC1005F24R9CS	1276-3904-1-ND
15	1	R15	Samsung Electro-Mechanics America, Inc	RES 18 OHM 1/16W 1% 0402	RC1005F180CS	1276-3893-1-ND
16	1	R18	Samsung Electro-Mechanics	RES 8.2 OHM 1/16W 1% 0402	RC1005F8R2CS	1276-3881-1-ND

17	3	AMP1,AMP2 AMP3	Skywork	IC AMP INGAP LF-9GHZ SC88	SKY65014-92LF	863-1262-1-ND
18	1	ATT	Skyworks	ATTENUATOR DGTL GAAS 6BIT QFN-24	SKY12347-362LF	863-1298-1-ND
19	8	S1,S2,S3,S4,S5,S6,S7,S8	Skyworks	IC SWITCH SPDT 100M-6GHZ 16-QFN	SKY13286-359LF	863-1049-1-ND

*The same name identification in Fig. 30 and 31.

3.2 Host test board and operational states

Fig. 33 shows the host test board the TTD version A. The TTD can be mounted onto the host test board using conventional solder reflow of BGA attachment. The label and operational states of the true time delay circuit version A is shown in Table 6. Table 7 shows the operational states for the attenuator. Fig. 34 shows the schematic diagram of the BGA test fixture.

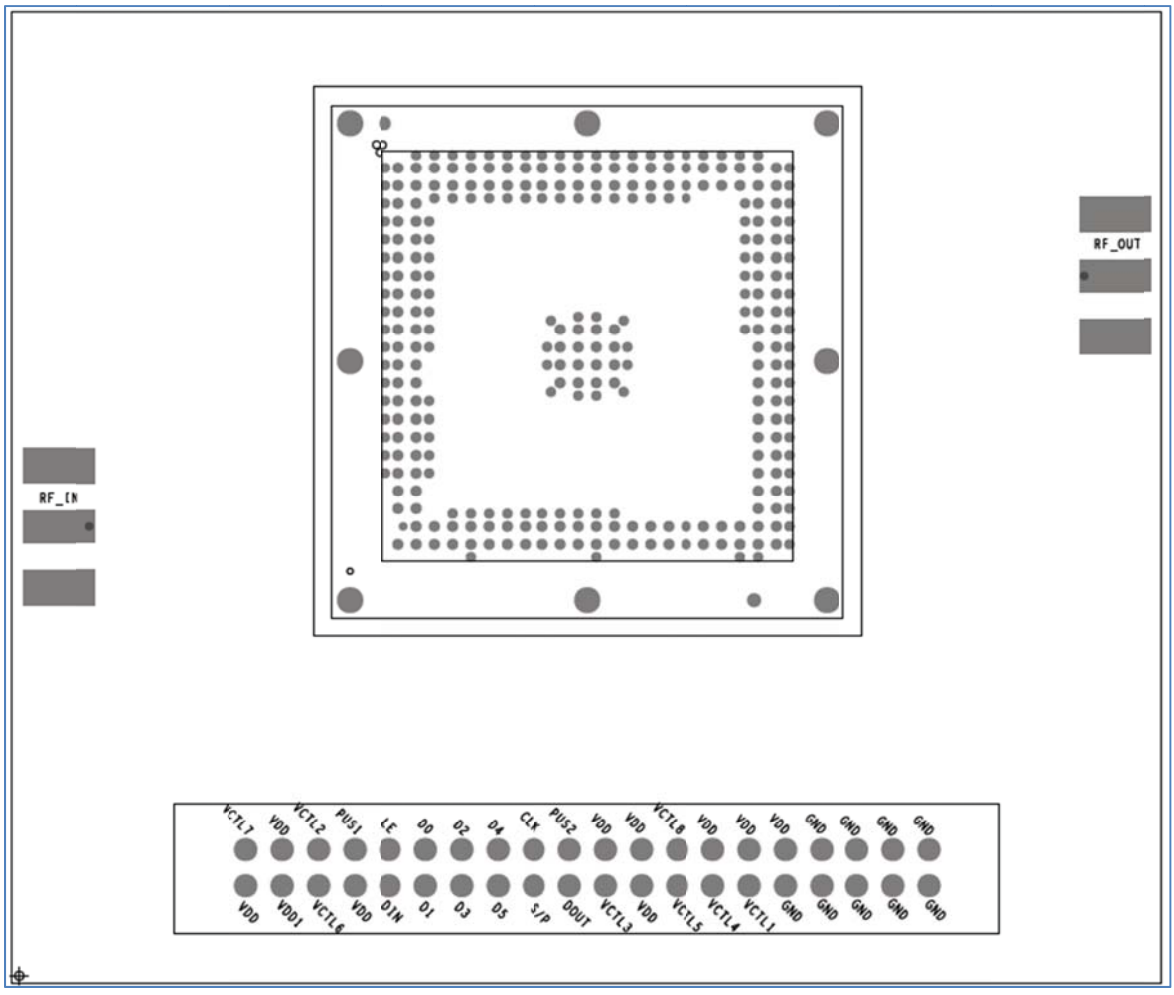


Fig. 33 Bottom view of the true time delay circuit version A

Table 6. Operational states of 8 switches of the true time delay circuit version A

Time delay (ns)	**VCTL1**	**VCTL2**	**VCTL3**	**VCTL4**	**VCTL5**	**VCTL6**	**VCTL7**	**VCTL8**
No delay	1	0	1	0	1	0	0	1
0.5	1	0	0	1	1	0	0	1
1.0	0	1	1	0	1	0	0	1
1.5	0	1	0	1	1	0	0	1
2.0	1	0	1	0	0	1	0	1
2.5	1	0	0	1	0	1	0	1
3.0	0	1	1	0	0	1	0	1
3.5	0	1	0	1	0	1	0	1
4.0	1	0	1	0	1	0	1	0
4.5	1	0	0	1	1	0	1	0
5.0	0	1	1	0	1	0	1	0
5.5	0	1	0	1	1	0	1	0
6.0	1	0	1	0	0	1	1	0
6.5	1	0	0	1	0	1	1	0
7.0	0	1	1	0	0	1	1	0
7.5	0	1	0	1	0	1	1	0

Note: “1” = high control voltage: +3.0 to VDD. “0” = low control voltage: 0 to +0.8 V.

Table 7. Operational states of 8 switches of the true time delay circuit version A

Attenuation level	**D5 (MSB)**	**D4**	**D3**	**D2**	**D1**	**D0 (LSB)**
Insertion loss	1	1	1	1	1	1
0.5 dB	1	1	1	1	1	0
1.0 dB	1	1	1	1	0	1
2.0 dB	1	1	1	0	1	1
4.0 dB	1	1	0	1	1	1
8.0 dB	1	0	1	1	1	1
16 dB	0	1	1	1	1	1
31.5 dB	0	0	0	0	0	0

Note: "1" = high control voltage: +3.0 to VDD. "0" = low control voltage: 0 to +0.8 V.

Note: VDD must apply before any control voltage.

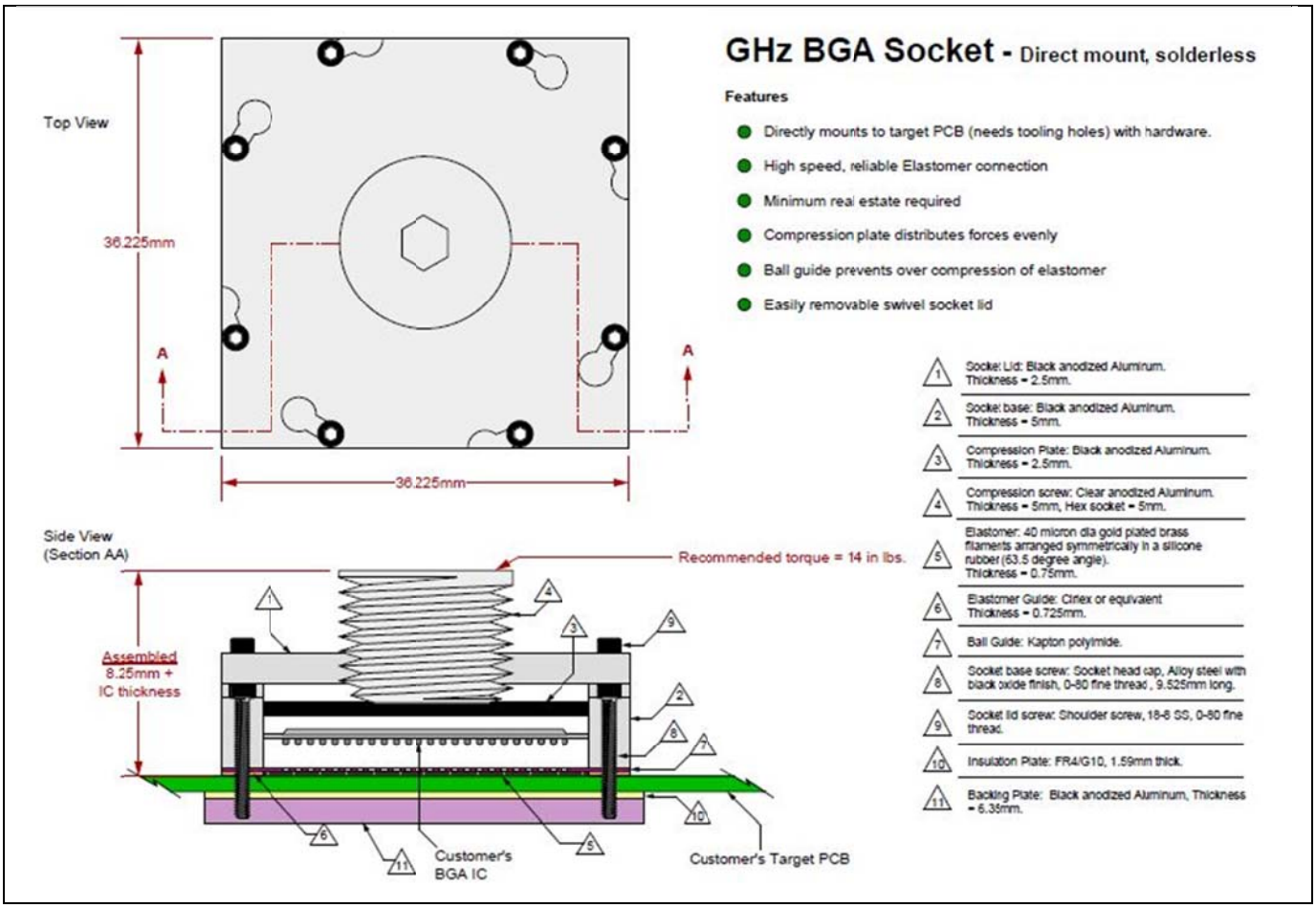


Fig. 34 Images of the 8GHz BGA socket

IV. Publication

V. L. Duong, A.-V. Pham, T. W. Dalrymple, M. Schadt, and C. L. Palomaki, "Development of a compact true time delay circuit," in Proceedings of GOMAC, Las Vegas, NV, March 2013.

V. Future Work

The surface mount passive devices have significant variations which cause significant degradation to the amplitude compensation networks and gain flatness. At this point, we tune and randomly select passive components that can provide the best gain flatness. Hence, it would be an advantage to combine gain stages, compensation networks, and other circuitry onto a single Si CMOS chip. The design of gain and amplitude compensation on a single Si CMOS chip with the delay on board is the direction of the future work. This would provide consistent phase and electrical performance as well as miniaturization.

VI. Appendix

1. Data sheet for the amplifier SKY65014
2. Data sheet for the switch SKY13286
3. Data sheet for the attenuator SKY12347

DATA SHEET

SKY65014-70LF: 0.1-7.0 GHz InGaP Cascadable Amplifier

Applications

- Wireless infrastructure: WLAN, HLAN, DBS, broadband, cellular base stations
- Test instrumentation
- Cable television

Features

- Broadband frequency range: 0.1 to 6.0 GHz
- Small signal gain = 16 dB typical @ 2 GHz
- High OIP3: +36 dBm typical
- OP1dB = +18 dBm typical @ 2 GHz
- Input and output impedance: 50 Ω nominal
- Single, positive DC supply voltage
- SOT-89 (4-pin, 1.5 x 4.0 mm) package (MSL1, 260 °C per JEDEC J-STD-020)

Skyworks Green™ products are compliant with all applicable legislation and are halogen-free. For additional information, refer to *Skyworks Definition of Green™*, document number SQ04-0074.

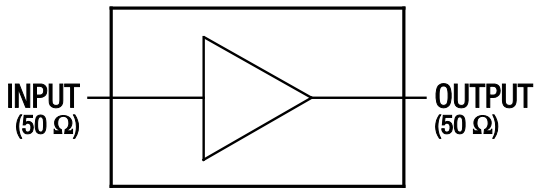


Figure 1. SKY65014-70LF Functional Block Diagram

Description

Skyworks SKY65014-70LF is a general purpose, broadband amplifier. The device is fabricated from Skyworks InGaP HBT process and packaged in a miniature Small Outline Transistor (SOT-89) package.

The device's 50 Ω input and output impedance allow it to be easily cascaded without external impedance matching networks. The typical –3 dB bandwidth of the SKY65014-70LF is 0.1 to 6.0 GHz.

The amplifier is also available in a plastic micro-X package (SKY65014-214LF) and an SC-88 package (SKY65014-92LF).

A functional block diagram is provided in Figure 1. The device package and pinout are shown in Figure 2.

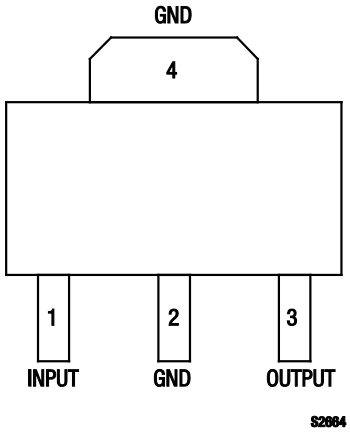


Figure 2. SKY65014-70LF Pinout – 4-Pin SOT-89 Package (Top View)

Electrical and Mechanical Specifications

Signal pin assignments and functional pin descriptions are described in Table 1. The absolute maximum ratings of the SKY65014-70LF are provided in Table 2. Electrical specifications are provided in Table 3.

Typical performance characteristics of the SKY65014-70LF are illustrated in Figures 3 through 6.

Table 1. SKY65014-70LF Signal Descriptions

Pin #	Name	Description
1	INPUT	RF input with 50 Ω nominal input impedance. An internally generated DC voltage is present at this pin, so an external DC block should be used to connect this pin to the external circuit.
2	GND	Ground
3	OUTPUT	RF output. DC supply voltage input and RF output with 50 Ω nominal output impedance. The nominal voltage required at this pin is listed in Table 3. Supply current is determined by an external resistor connected between the DC power supply and this pin.
4	GND	Ground

Table 2. SKY65014-70LF Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units
Supply voltage	V_{DD}		5	V
RF input power	P_{IN}		+15	dBm
Supply current	I_{DD}		120	mA
Power dissipation @ T_C = 25 °C	P_D		600	mW
Operating case temperature	T_C	–40	+85	°C
Storage temperature	T_{ST}	–65	+125	°C
Junction temperature	T_J		+150	°C
Thermal resistance	Θ_{JC}		70	°C/W

Note: Exposure to maximum rating conditions for extended periods may reduce device reliability. There is no damage to device with only one parameter set at the limit and all other parameters set at or below their nominal values. Exceeding any of the limits listed here may result in permanent damage to the device.

***CAUTION**: Although this device is designed to be as robust as possible, Electrostatic Discharge (ESD) can damage this device. This device must be protected at all times from ESD. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD precautions should be used at all times.*

Table 3. SKY65014-70LF Electrical Specifications (Note 1)
(I_{DD} = 70 mA, T_C = 25 °C, P_{IN} = 0 dBm, Characteristic Impedance [Z_O] = 50 Ω, Unless Otherwise Noted)

Parameter	Symbol	Test Conditions	Min	Typical	Max	Units
Small signal gain	|S21|	@ 2 GHz	15	16	17	dB
3 dB gain bandwidth	BW_{3DB}			6		GHz
Noise Figure	NF	@ 2 GHz		4.8		dB
1 dB Output Compression Point	OP1dB	@ 2 GHz	+17	+18		dBm
Input and output VSWR	VSWR	0.1 to 5.0 GHz		1.9:1	2.0:1	–
3rd Order Output Intercept Point	OIP3	@ 2 GHz, P_{IN} = 0 dBm/tone, Δf = 10 MHz		+36		dBm
Operating voltage	V_{DD}	Measured @ pin 3	4.2	4.7	5.0	V
Reverse isolation	|S12|	0.1 to 6.0 GHz		18		dB
Gain flatness		10 MHz to 6 GHz		±1.5		dB

Note 1: Performance is guaranteed only under the conditions listed in this Table.

Typical Performance Characteristics

(I_{DD} = 70 mA, Characteristic Impedance [Z_O] = 50 Ω, Unless Otherwise Noted)

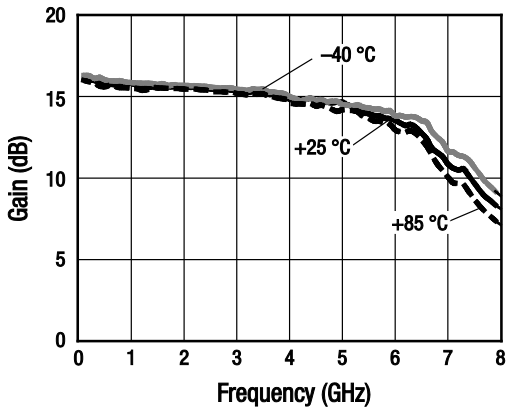


Figure 3. Small Signal Gain vs Frequency

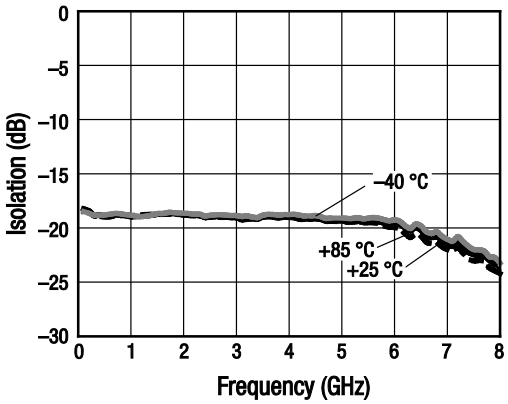


Figure 4. Isolation vs Frequency

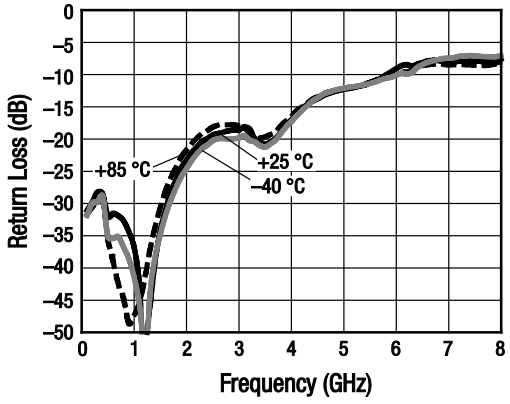


Figure 5. Input Return Loss vs Frequency

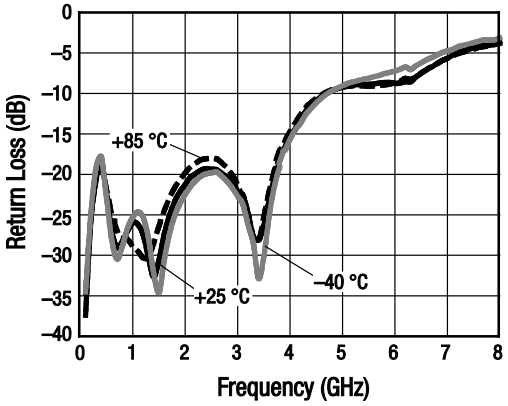


Figure 6. Output Return Loss vs Frequency

Evaluation Board Description

The Skyworks SKY65014-70LF Evaluation Board is used to test the performance of the SKY65014-70LF cascadable amplifier. The Evaluation Board is shown in Figure 7. An Evaluation Board schematic is shown in Figure 8. Table 4 provides the Bill of Materials (BOM) for Evaluation Board components.

The input and output of the SKY65014-70LF are connected using 50 Ω microstrip transmission lines with DC blocking capacitors, C1 and C2, to the input and output SMA connectors, respectively.

The positive supply voltage, V_{DD}, is connected to pin 3 (OUTPUT) of the amplifier using the decoupling network that consists of C4, L1, L2, and R1. The power supply current, I_{DD}, must be limited either by the current limit function of an external bench power supply or by replacing L3 with reistor R1, the value of which is given in shown in Table 5. The Evaluation Board is shipped with L3 in place, which shifts an in-band series resonance of the supply decoupling network out of band. For low frequency applications, R1 may be used to conveniently limit supply current on the Evaluation Board.

The Evaluation Board also contains a probe fixture that facilitates the direct measurement of the S-parameters. The probe fixture comprises a very short Co-Planar Waveguide (CPW) transmission line to pin 1 and an identical line to pin 3. The other two pins of the amplifier are grounded. The CPW transmission lines are compatible with ground-signal-ground wafer probe tips, which can be connected to the RF ports of a Vector Network Analyzer (VNA) using coaxial cables. The very small electrical length of these CPW transmission lines obviates the need to de-embed their effects from the S-parameters that are measured. The supply constant current must be applied using the bias tee, which is typically integrated into the VNA, and cascaded with the OUTPUT pin of the amplifier.

Package Dimensions

Typical case markings for the SKY65014-70LF are shown in Figure 9. The PCB layout footprint for the SKY65014-70LF is provided in Figure 10. Package dimensions for the 4-pin SOT-89 are provided in Figure 11, and tape and reel dimensions are shown in Figure 12.

Package and Handling Information

Instructions on the shipping container label regarding exposure to moisture after the container seal is broken must be followed. Otherwise, problems related to moisture absorption may occur when the part is subjected to high temperature during solder assembly.

The SKY65014-70LF is rated to Moisture Sensitivity Level 1 (MSL1) at 260 °C. It can be used for lead or lead-free soldering. For additional information, refer to the Skyworks Application Note, *Solder Reflow Information*, document number 200164.

Care must be taken when attaching this product, whether it is done manually or in a production solder reflow environment. Production quantities of this product are shipped in a standard tape and reel format.

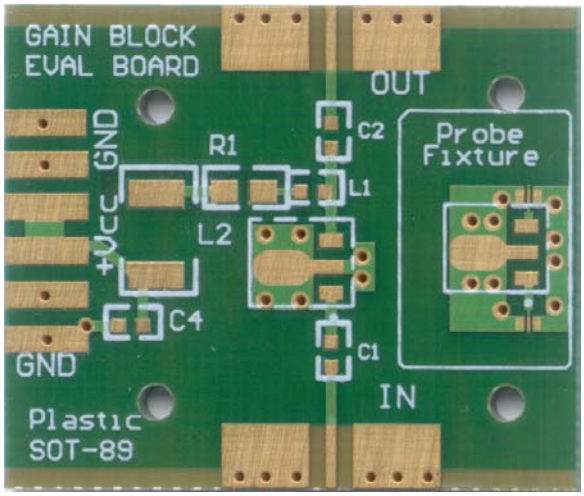


Figure 7. SKY65014-70LF Evaluation Board

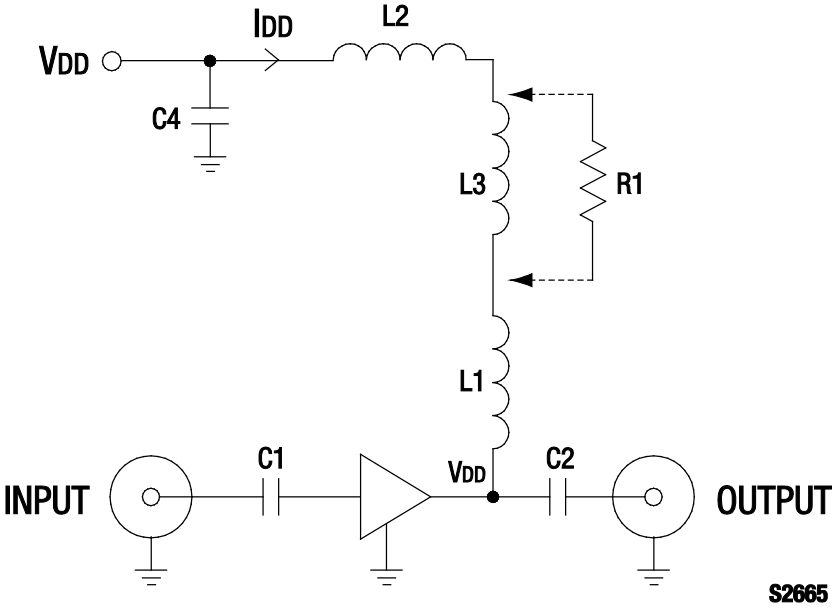


Figure 8. SKY65014-70LF Evaluation Board Schematic

Table 4. SKY65014-70LF Evaluation Board Bill of Materials (BOM)

Component	Value	Size	Part Number	Manufacturer
C1, C2, C4	47 nF	0603	GRM188R71E473K	Murata
L1	33 nH	0603	0603CS-33NX_LU	Coilcraft
L2	1600 Ω	1810	FBMH4525HM162N-T	Taiyo-Yuden
L3	110 nH	0805	0805CS-111X_L	Coilcraft
R1	See Table 5	0603	Variable	Variable

Table 5. Current Limiting Resistor Values

Supply Voltage (V)	Value of R1 (Ω)	Minimum Power Dissipation Rating (mW)
5.0	4	125
6.0	19	125
7.0	33	250
8.0	47	500
9.0	61	500
10.0	76	500
12.0	104	1000

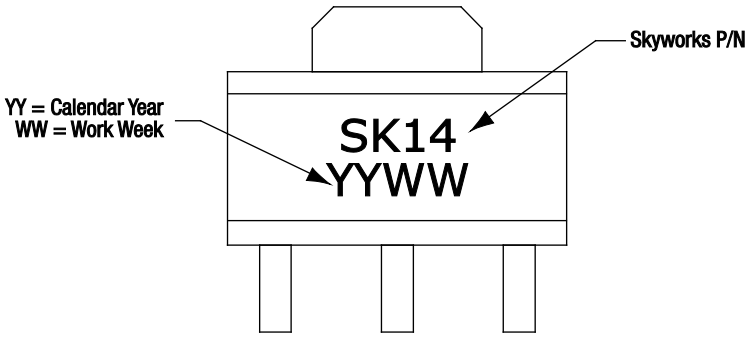


Figure 9. SKY65014-70LF Typical Case Markings

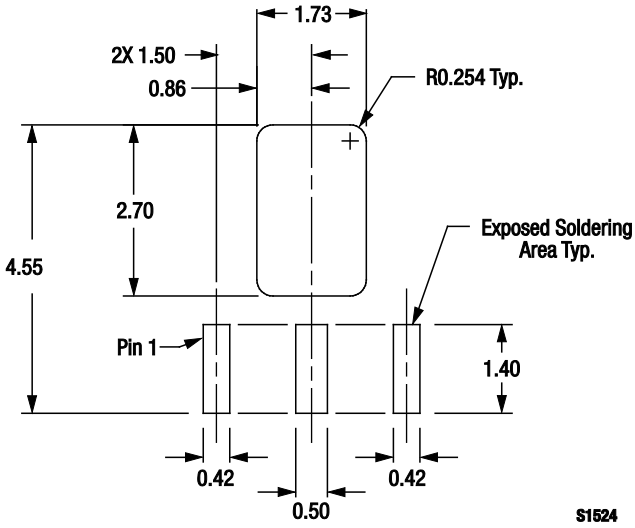
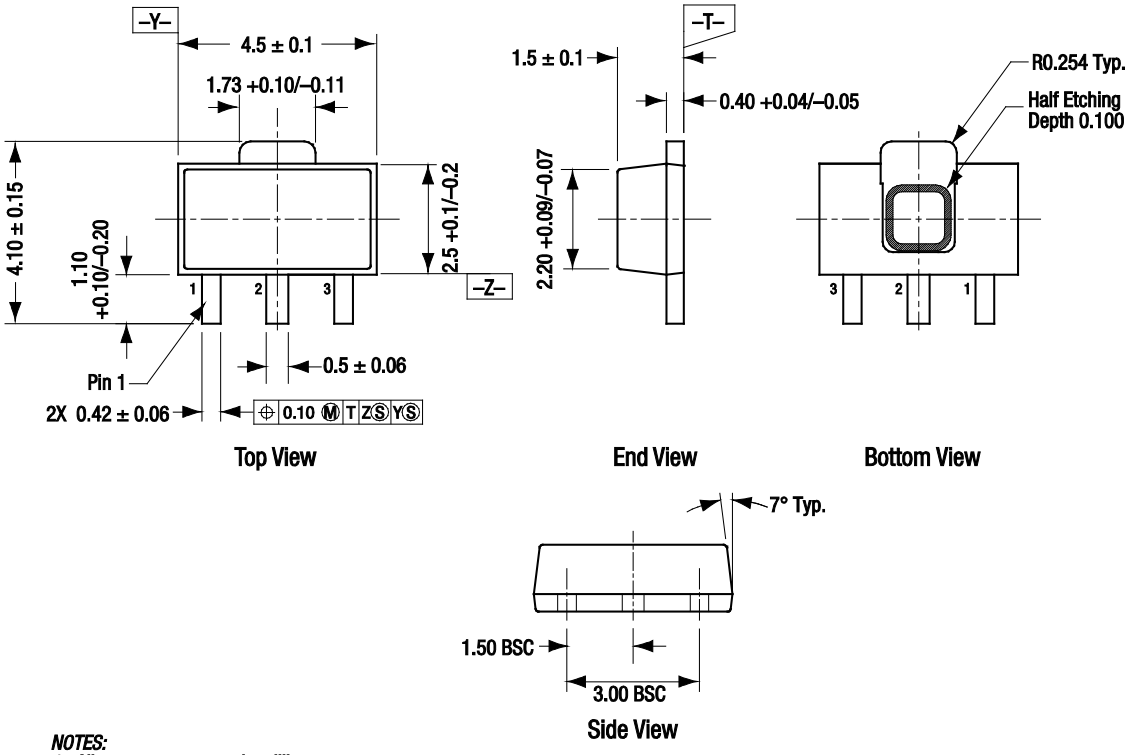


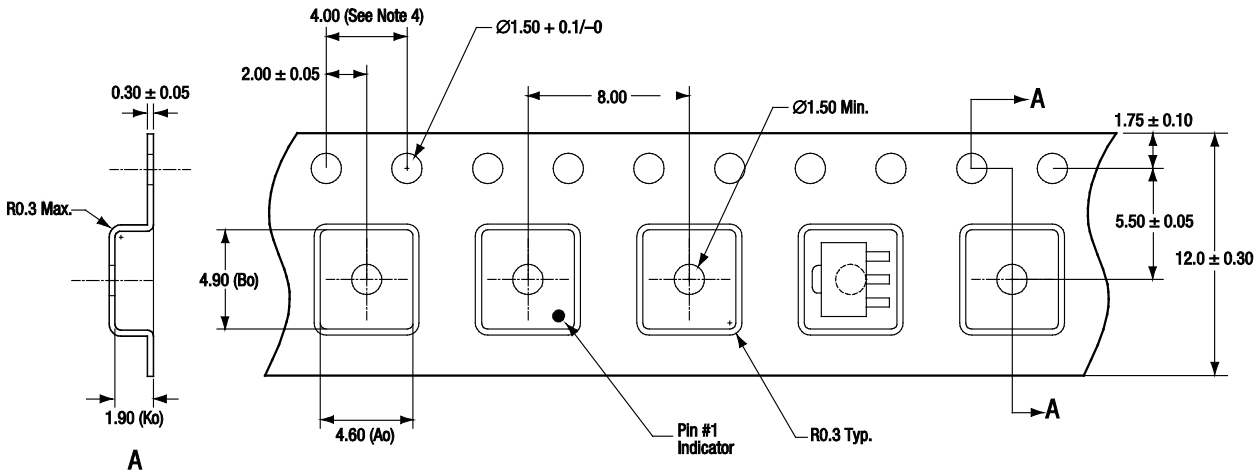
Figure 10. SKY65014-70LF PCB Layout Footprint



NOTES:
1. *All measurements are in millimeters.*
2. *Dimensioning and tolerancing according to ASME Y14.5M-1994.*
3. *Package dimension does not include mold protrusions or gate burrs. Mold protrusions and gate burrs do not exceed 0.005" per end. Body width dimension does not include interlead mold protrusions. Interlead protrusions do not exceed 0.005" per side.*
4. *Leadwidth dimension does not include dambar protrusions. Allowable protrusion does not exceed 0.002" total in excess of lead width dimension at maximum material condition.*

S2660

Figure 11. SKY65014-70LF 4-Pin SOT-89 Package Dimensions



Notes:
1. *Carrier tape material: black conductive polycarbonate or polystyrene.*
2. *Cover tape material: transparent conductive PSA.*
3. *Cover tape size: 9.2 mm width.*
4. *10 sprocket hole pitch cumulative tolerance: ± 0.2 mm*
5. *Ao and Bo measurement point to be 0.30 mm from bottom pocket.*
6. *All measurements are in millimeters.*

S2813

Figure 12. SKY65014-70LF Tape and Reel Dimensions

Development of a Compact True Time Delay Circuit

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Endicott, N.Y. 13760.

GOMAC 2013

Outline

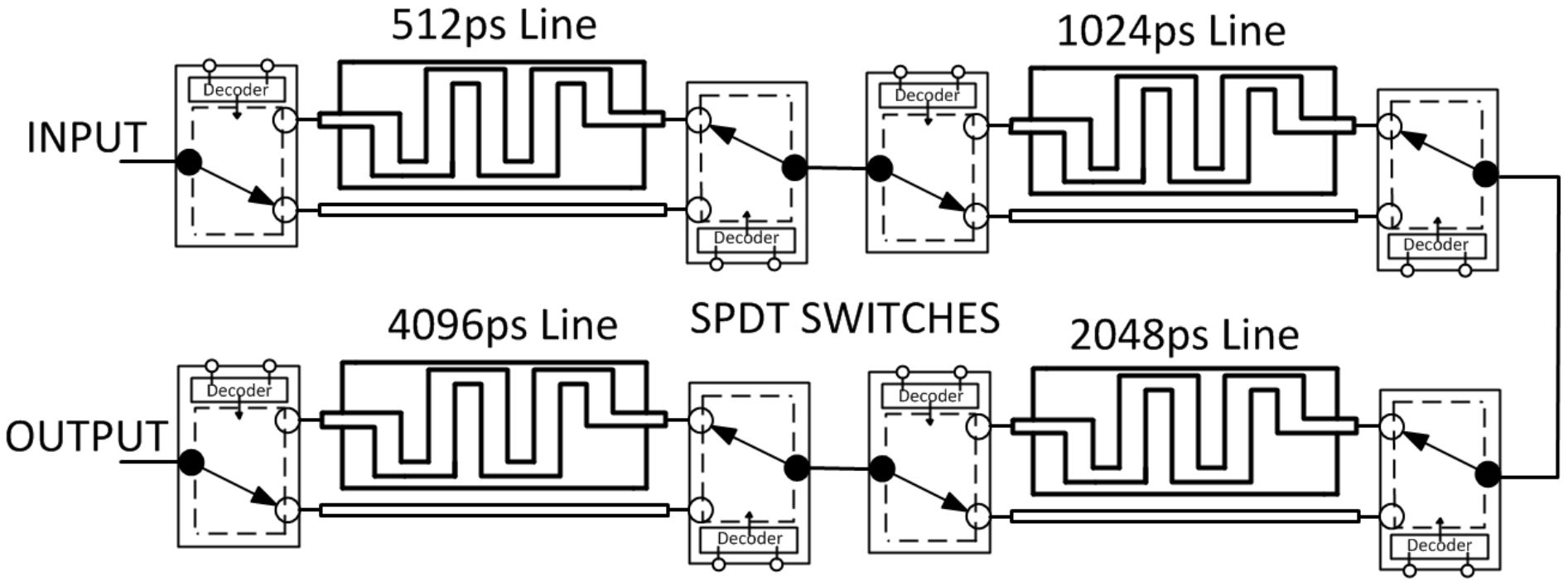
- Motivation
- Proposed True Time Delay Package
- Design and Simulation of the TTD Package
- Fabrication and Prototype of the TTD Package
- Measurement Results
- Proposed Amplitude-Compensated TTD Package
- Conclusion

Motivations

- True time delay circuits are used for wide bandwidth beam steering of phased array antennas
- Long delay is needed for large steering angles, large arrays, wide instantaneous bandwidth, and low frequency arrays.
- Integrated circuit approaches can be costly and are typically limited to less than 1 ns
- TTD modules can provided multiple ns of delay

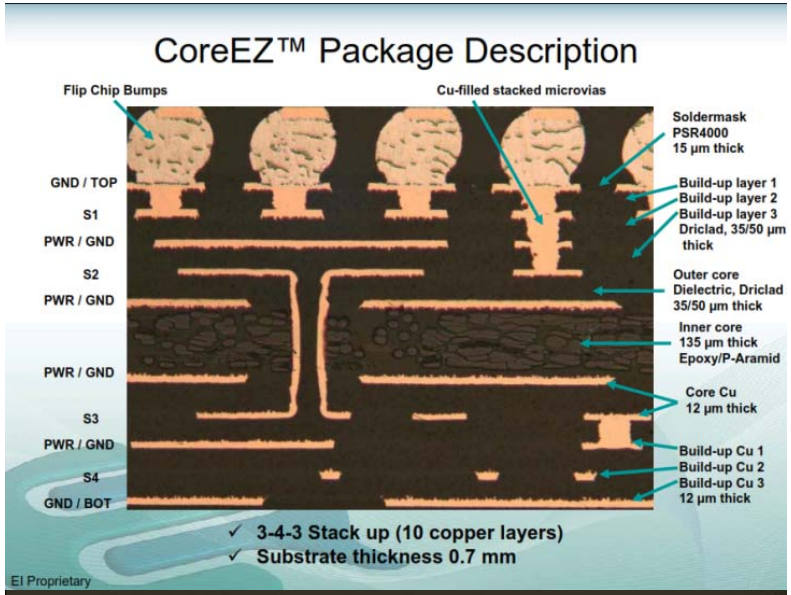
Proposed TTD Module

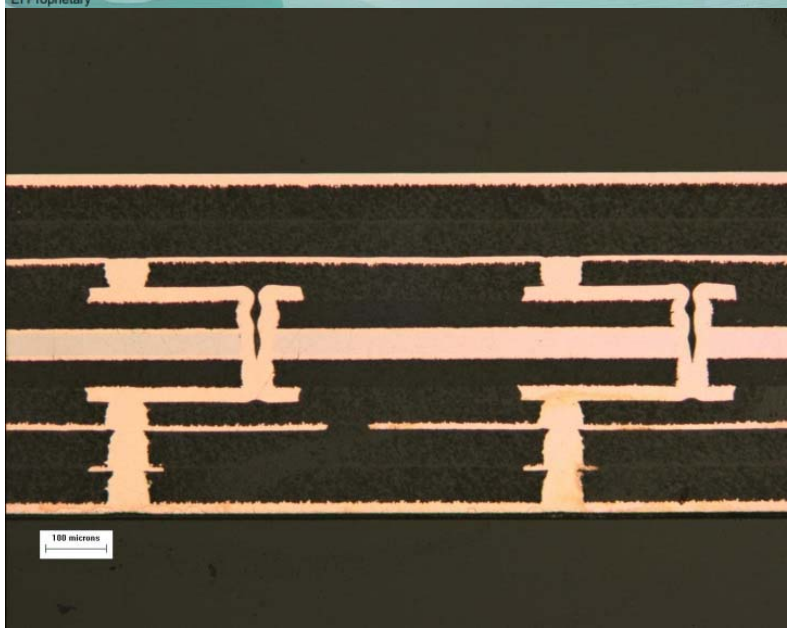
- **Develop a 4-bit TTD module with a total delay of 7.5 ns from 0.3 to 3 GHz**
- **The TTD built in a BGA multi-layered package with commercially available switches**

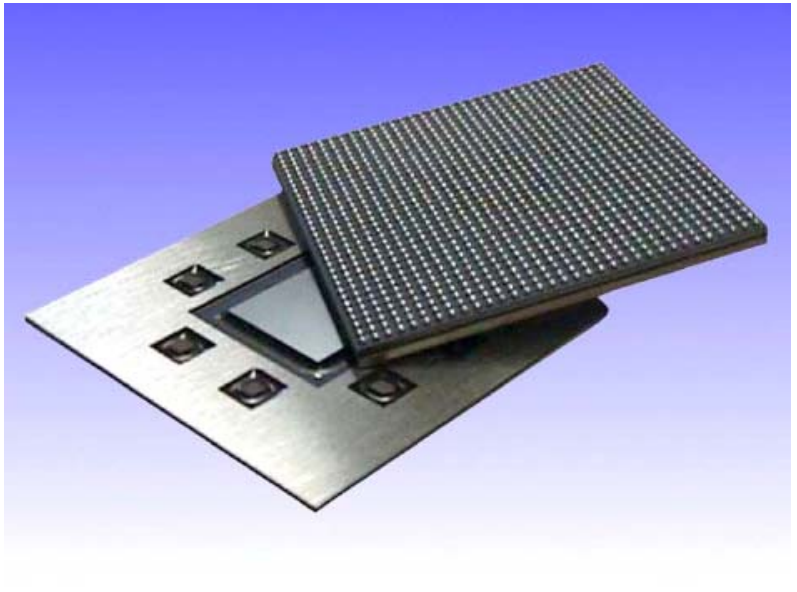


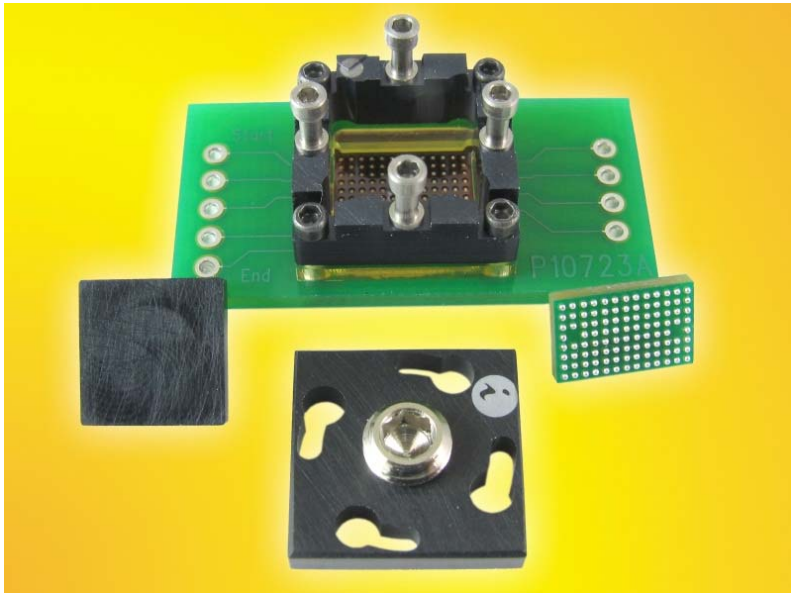
True Time Delay Circuit

HyperBGA Technologies









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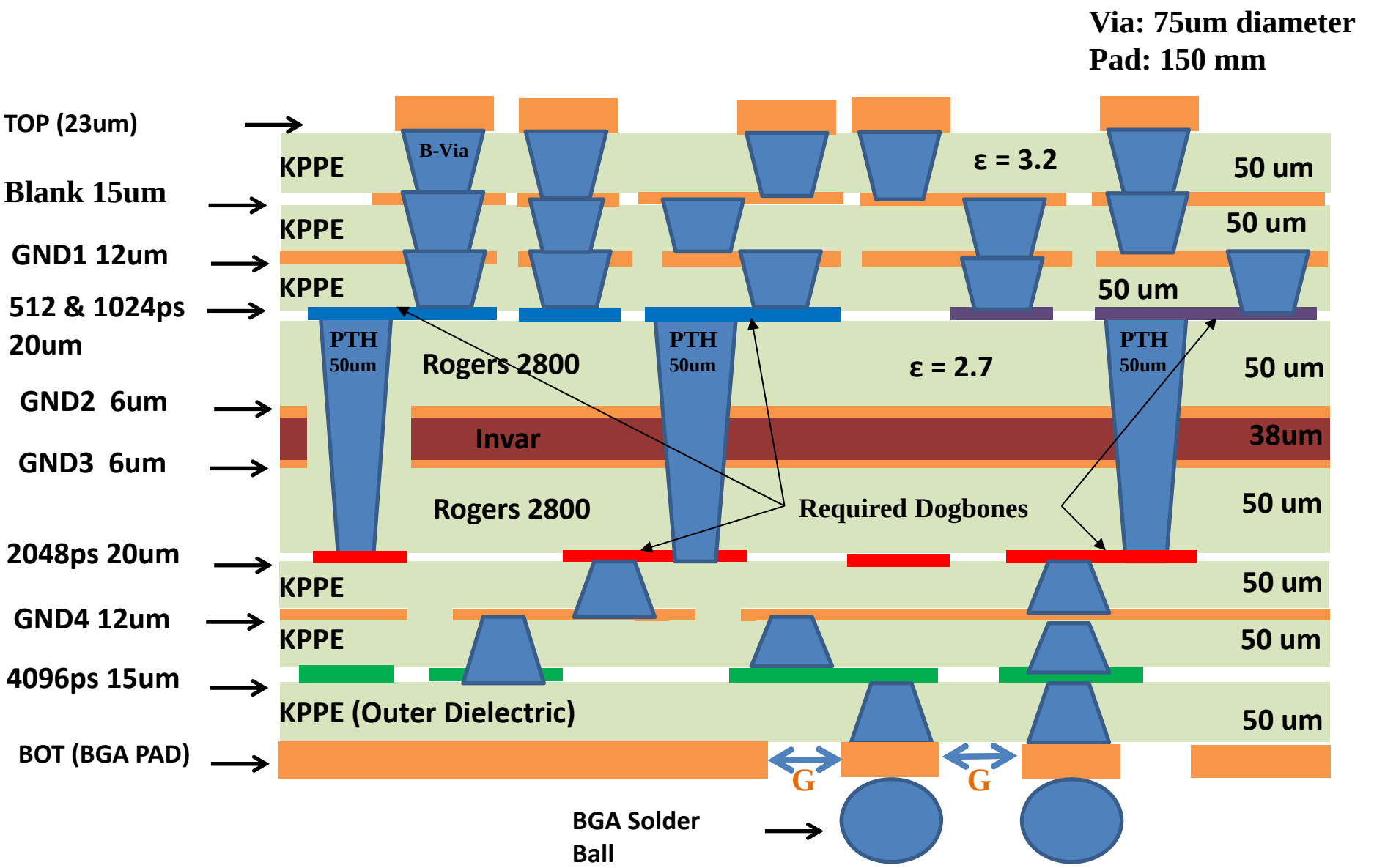
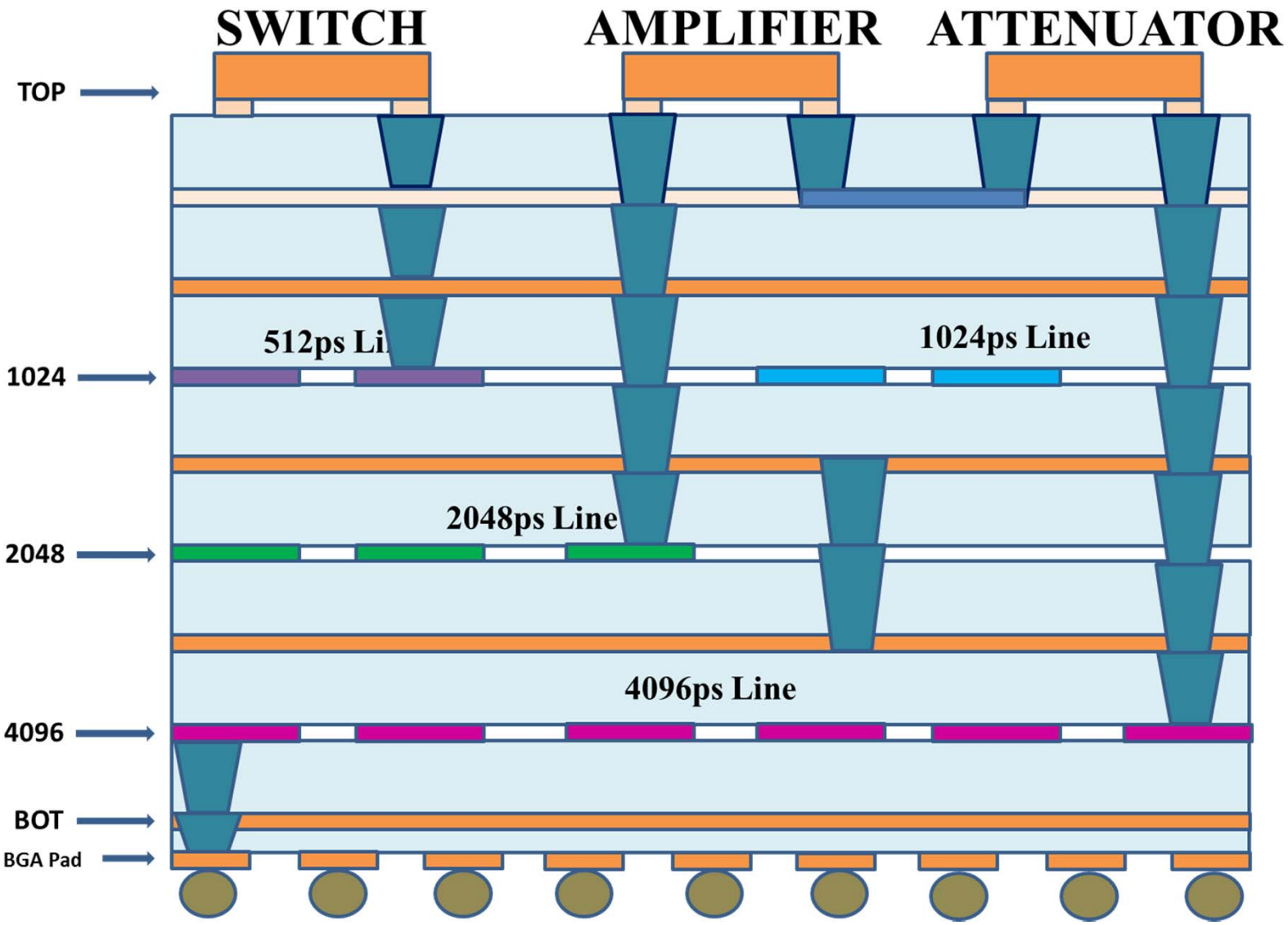
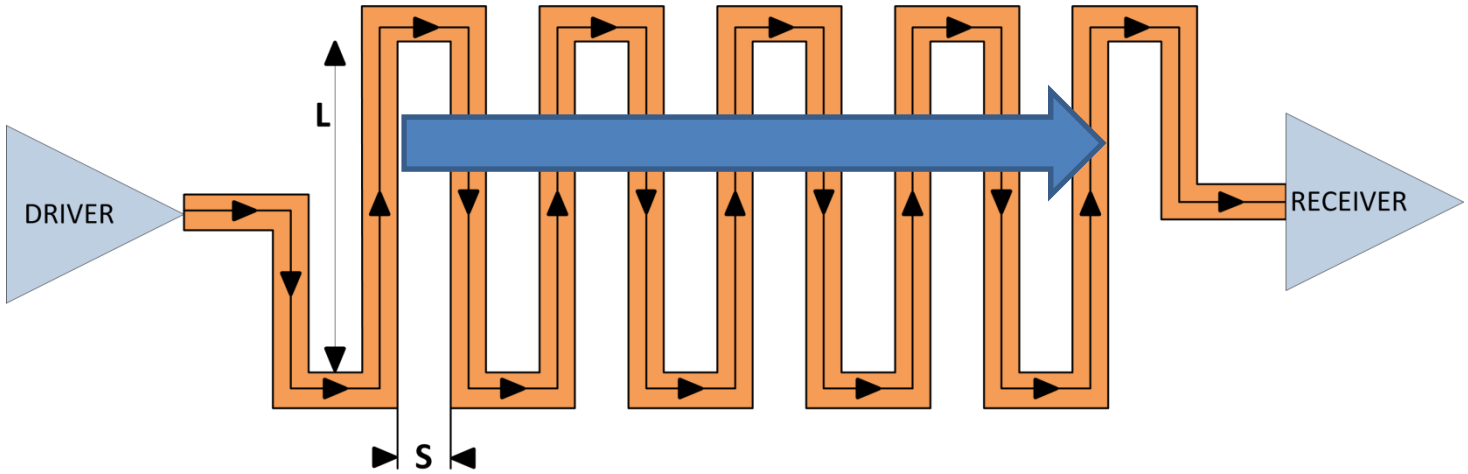
Proposed HyperBGA X-section



Partition of Delayed Lines



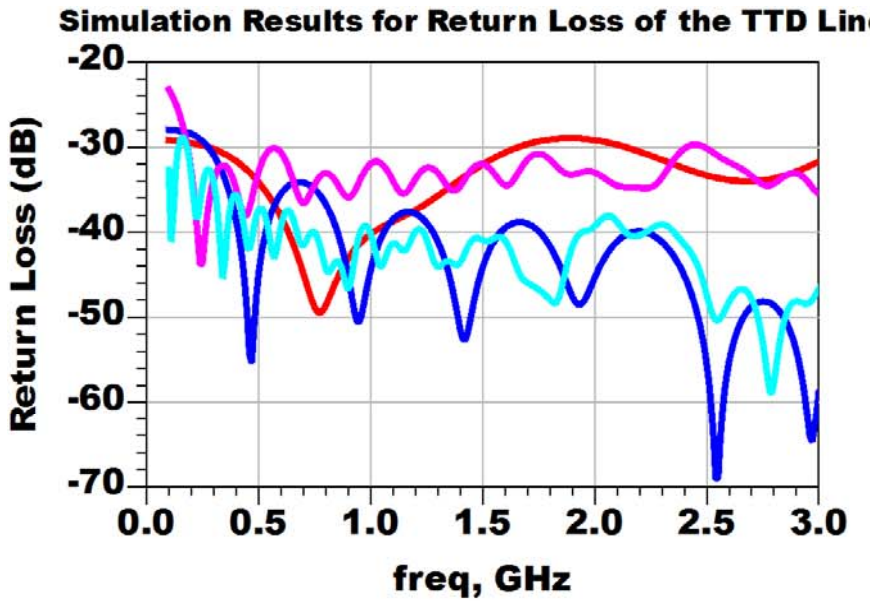
Meander Line Analysis

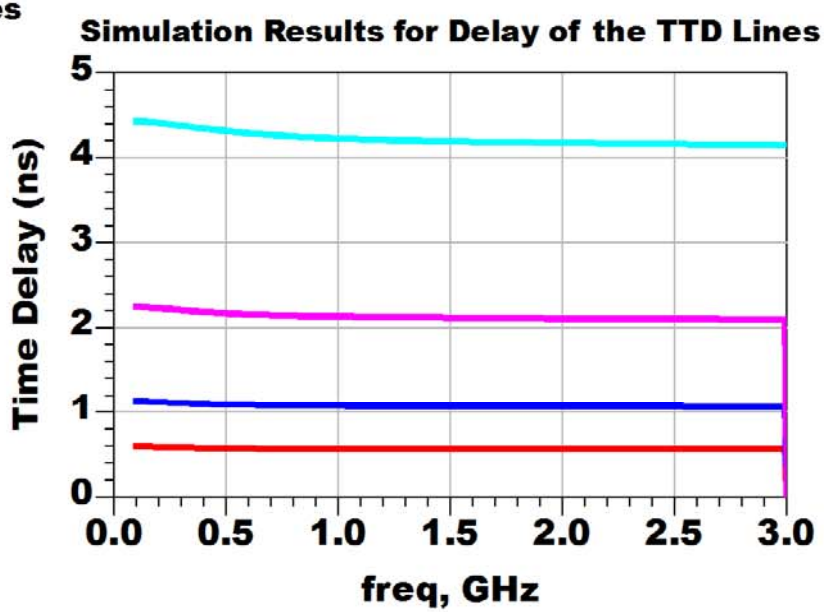


- Mutual inductance, and coupling capacitor, and impedance matching cause shift in delay from a typical straight transmission line

- To minimize the effect:
  - ✓ Spacing between two adjacent line (S) proportional to the coupling
  - ✓ Length (L) of the line also proportional to the coupling

HFSS Simulation of Delayed Lines



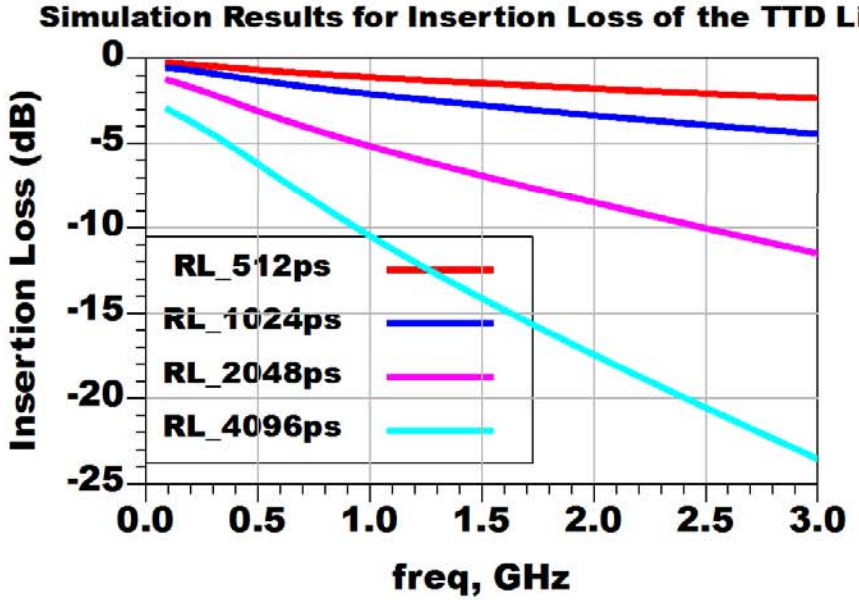


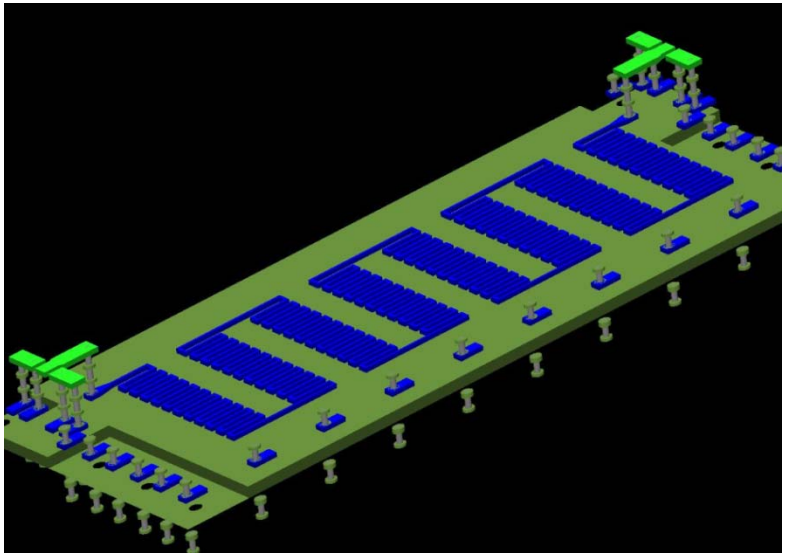
4148ps

2095ps

1063ps

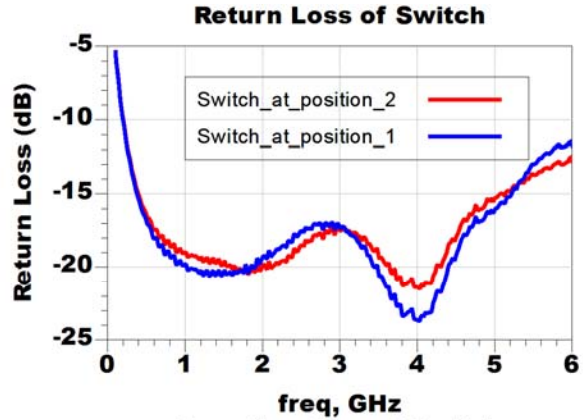
557ps

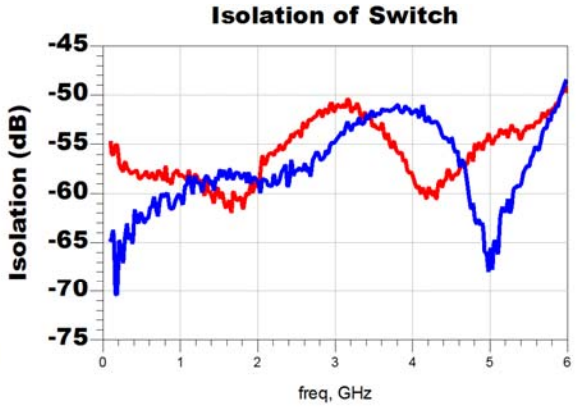


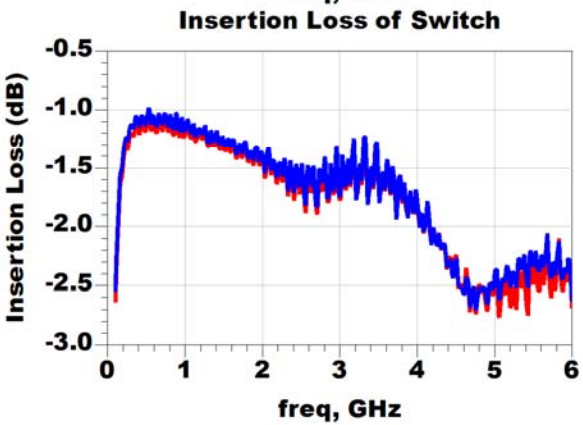


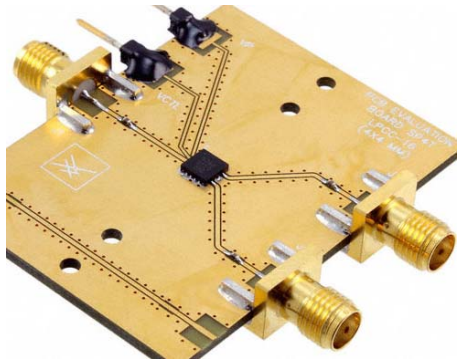
Commercially Available Switches

- The SKY13286-359LF is a GaAs pHEMT FET high-isolation and absorptive switch
- The switch is provided in a 4 x 4 mm, 16-pin Quad Flat No-Lead (QFN) package
- Single, positive voltage control: 0 to 3 V and 0 to 5 V
- High isolation of 55 dB at 0.1 GHz and 3 GHz









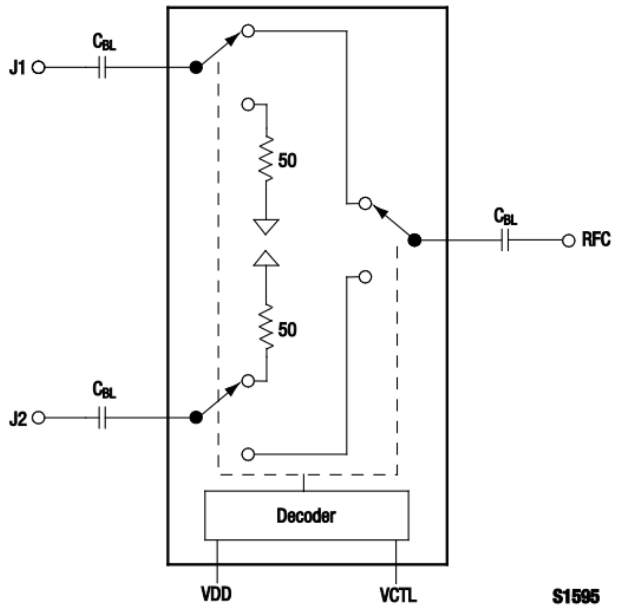
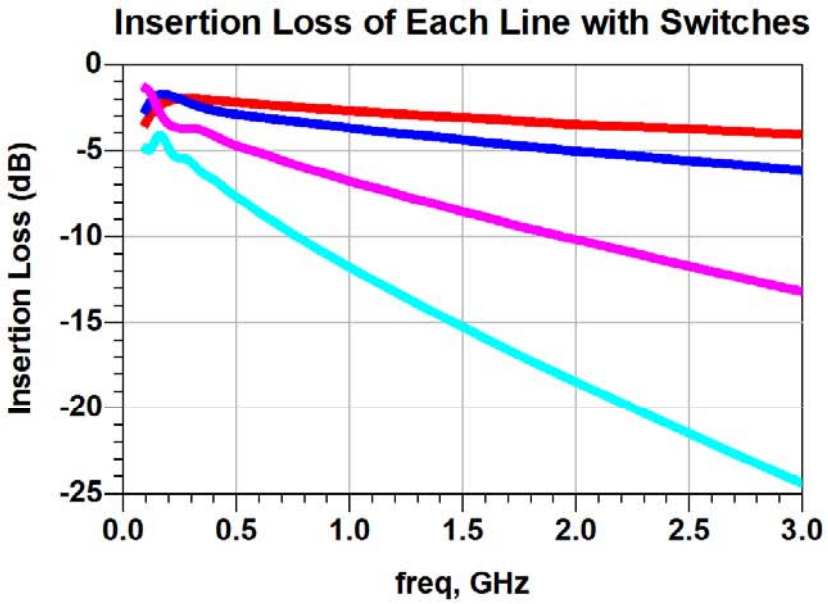
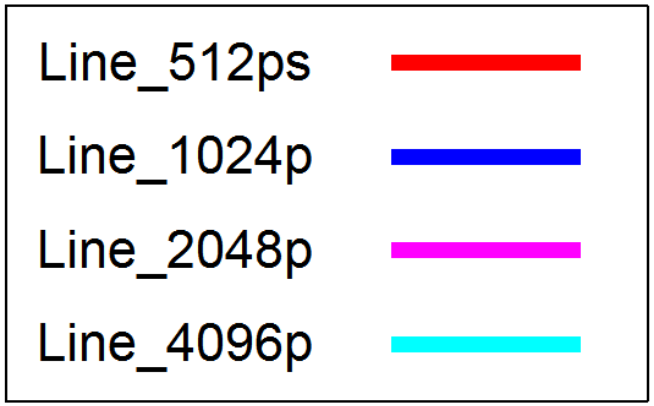


Figure 1. SKY13286-359LF Block Diagram

Measurements of Cascaded Delay Lines and Switches





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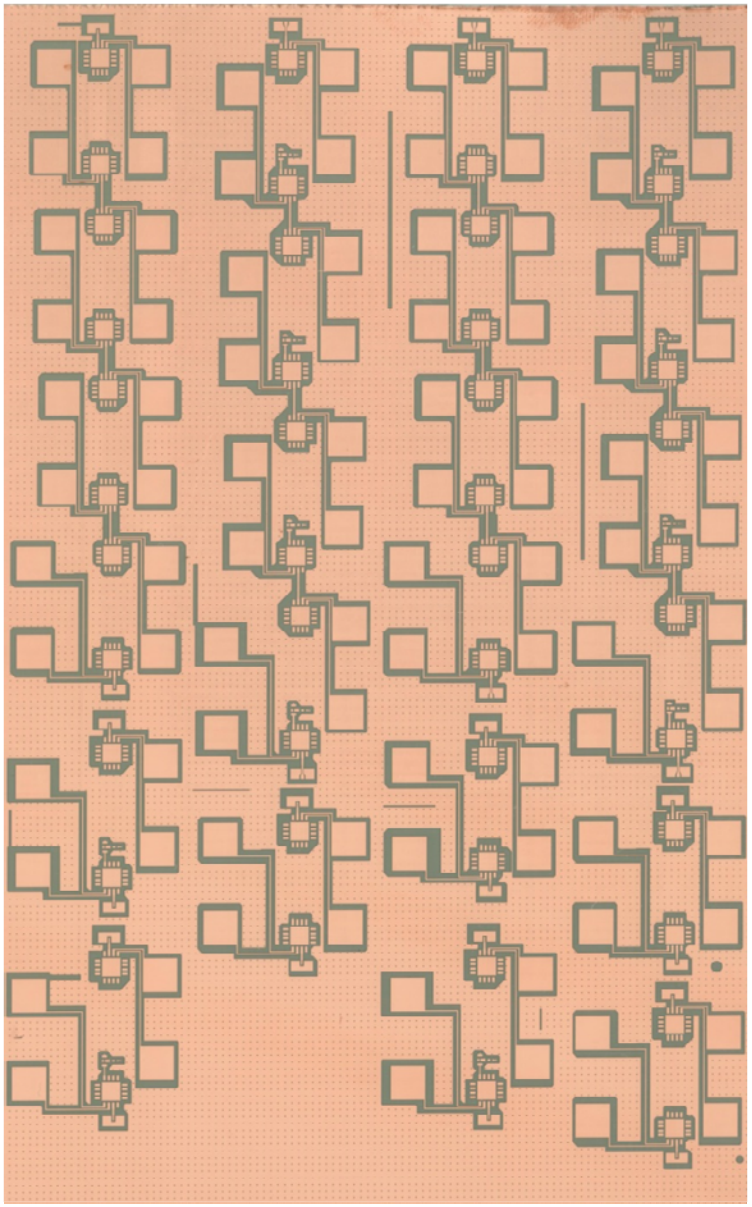
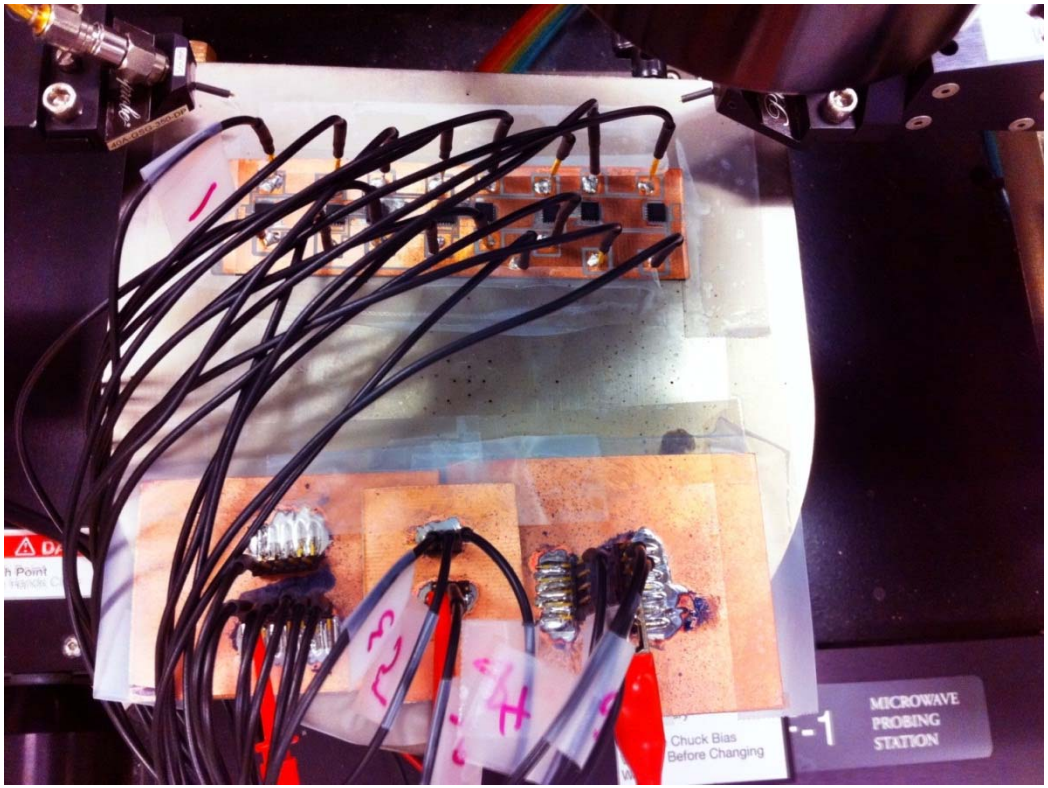
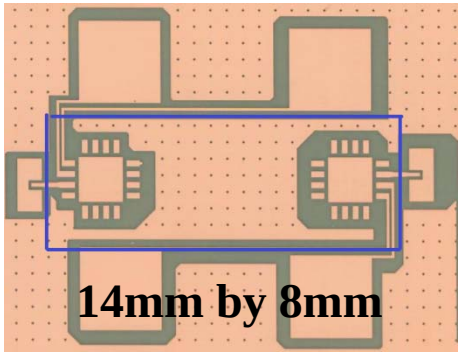
HyperBGA Prototypes





Testing the TDU with FPGA Control On-wafer measurement



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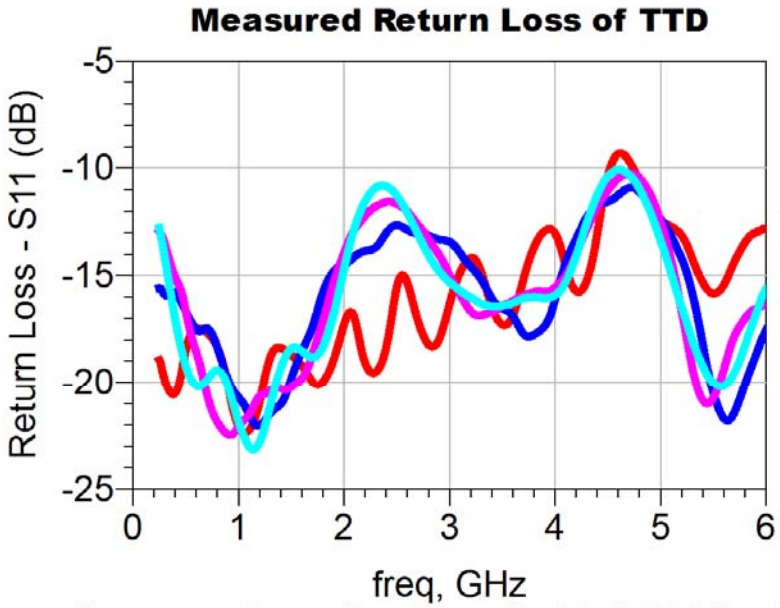
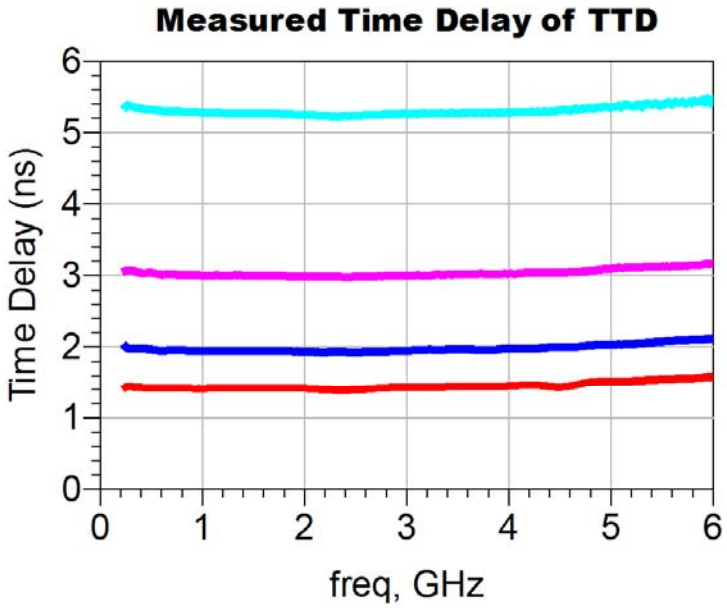
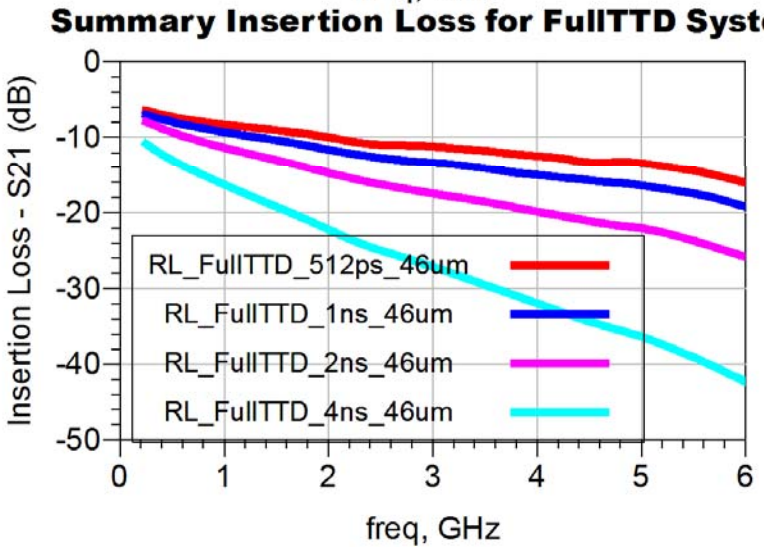
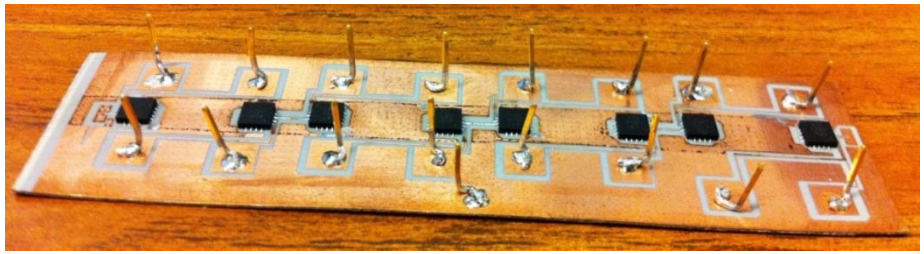
Measurements of the TTD Prototype





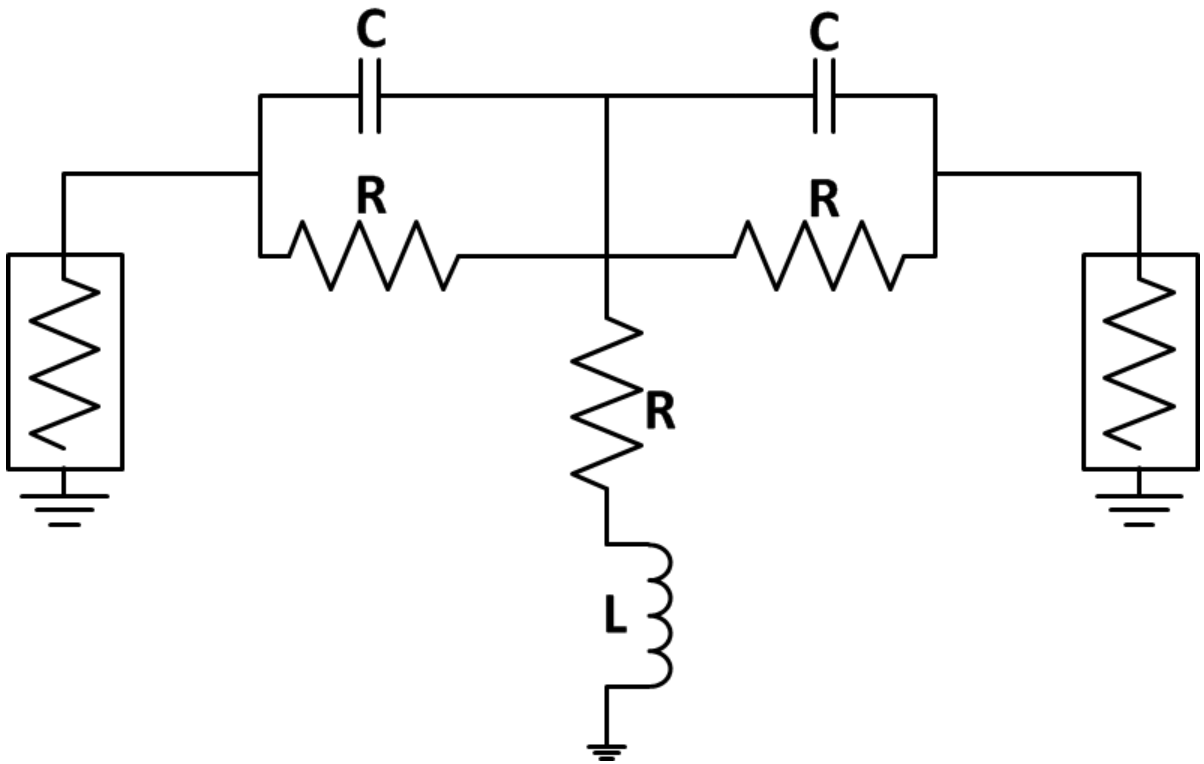




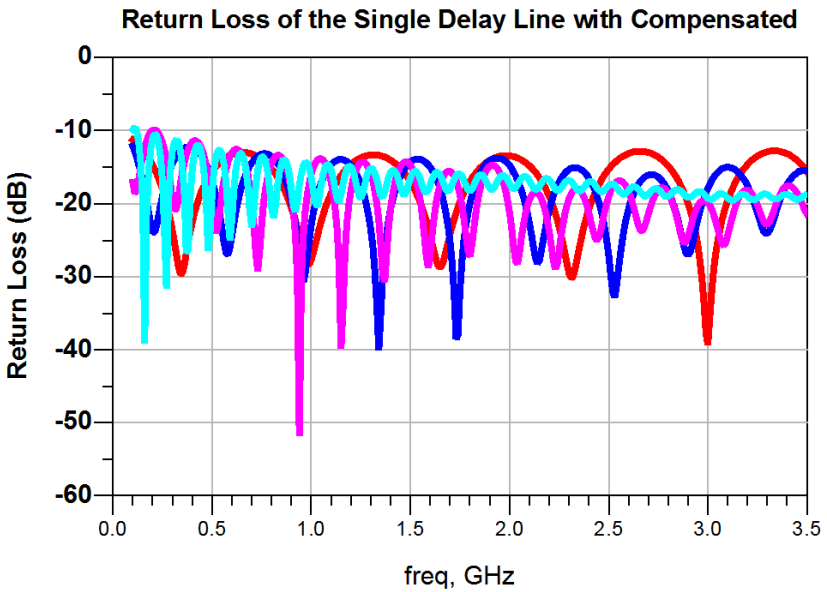
Un-folded TTD for Measurement

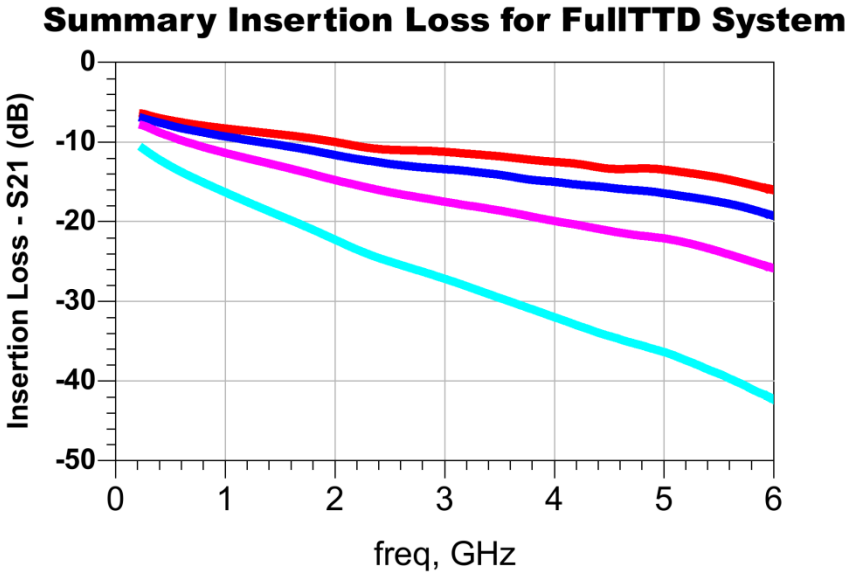
Amplitude-Compensated Circuits

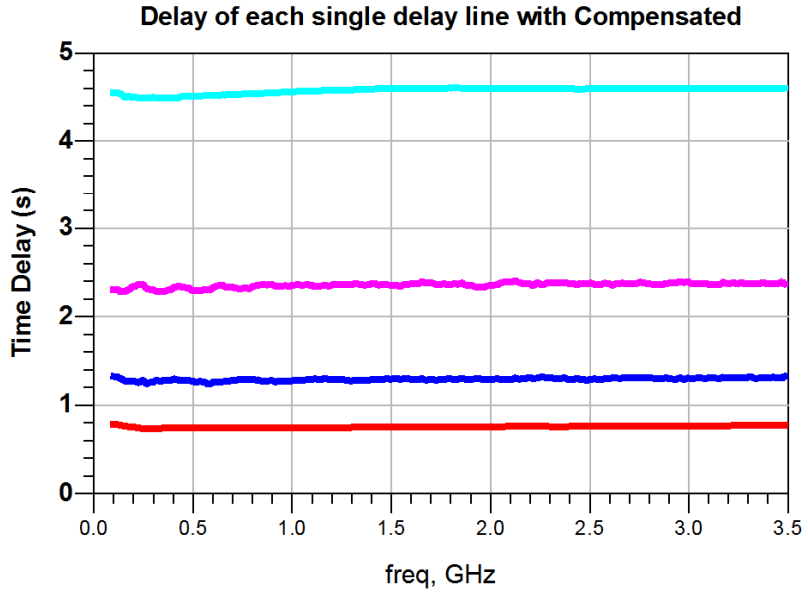
- **High Pass Filter with Attenuator to achieve slope compensation**

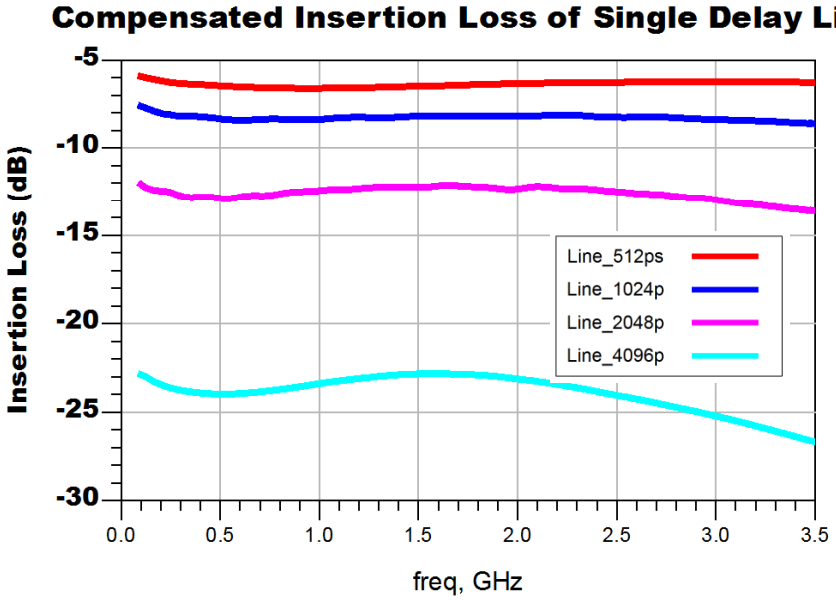


Before and After Compensated for TTD

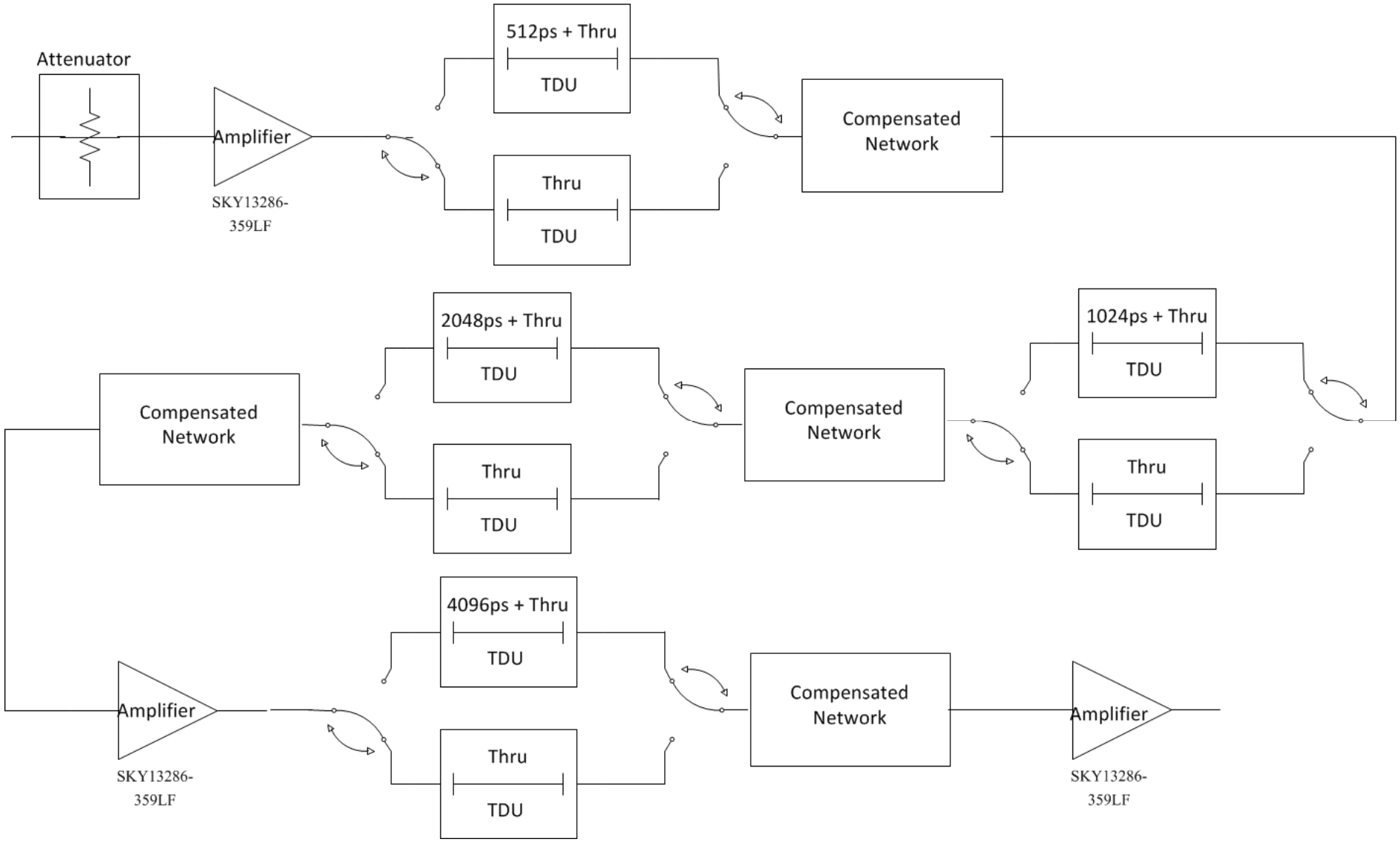




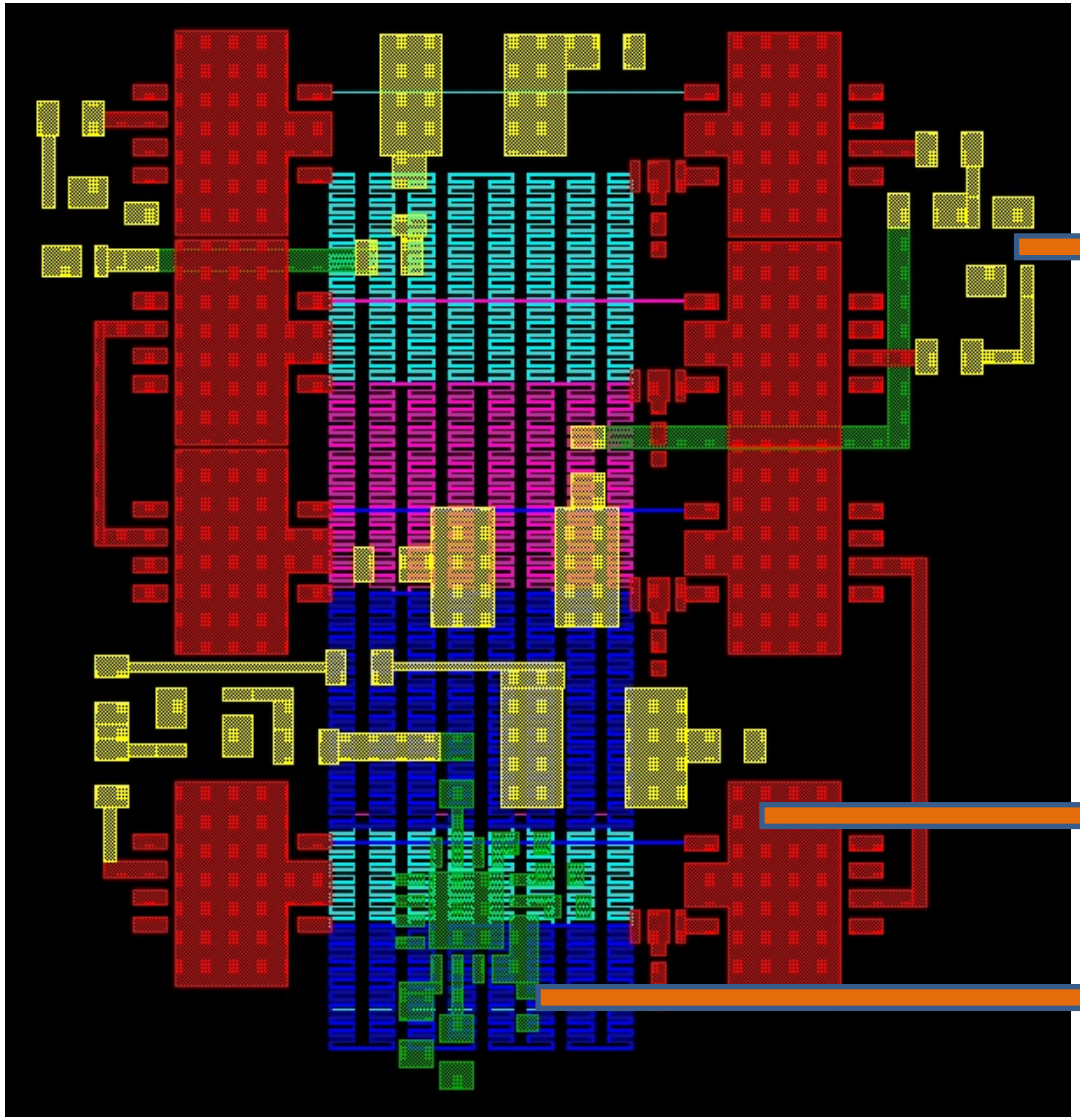




Full TTD with Compensated Network



Layout of TTD with Compensated Network



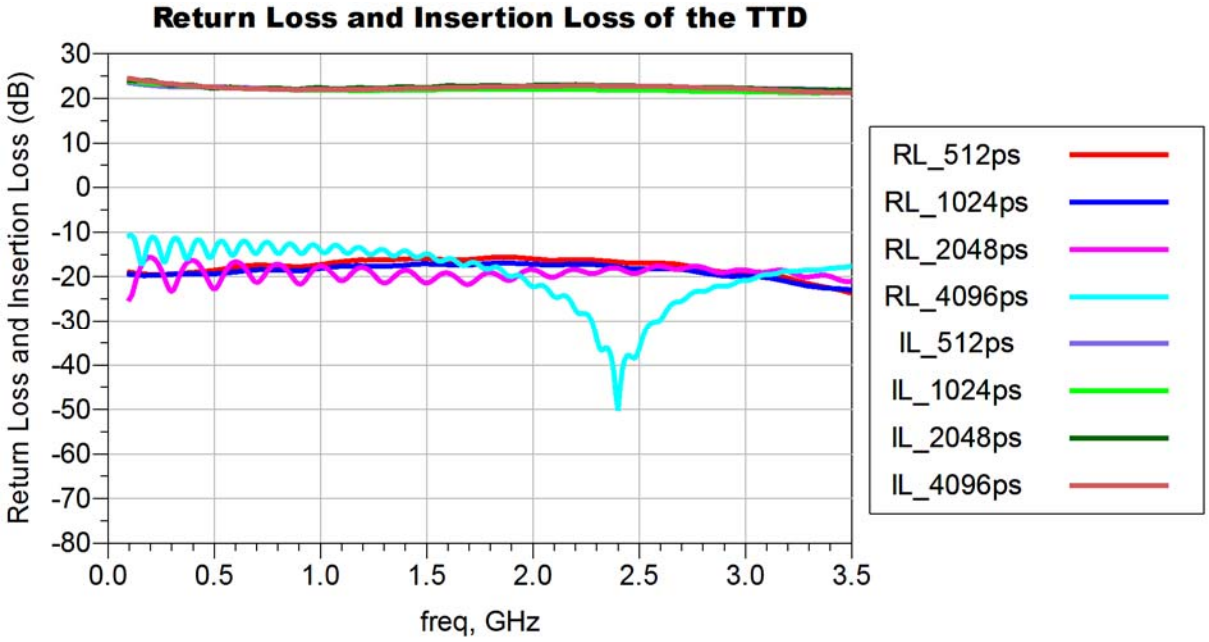
Size 1.5in by 1.5in

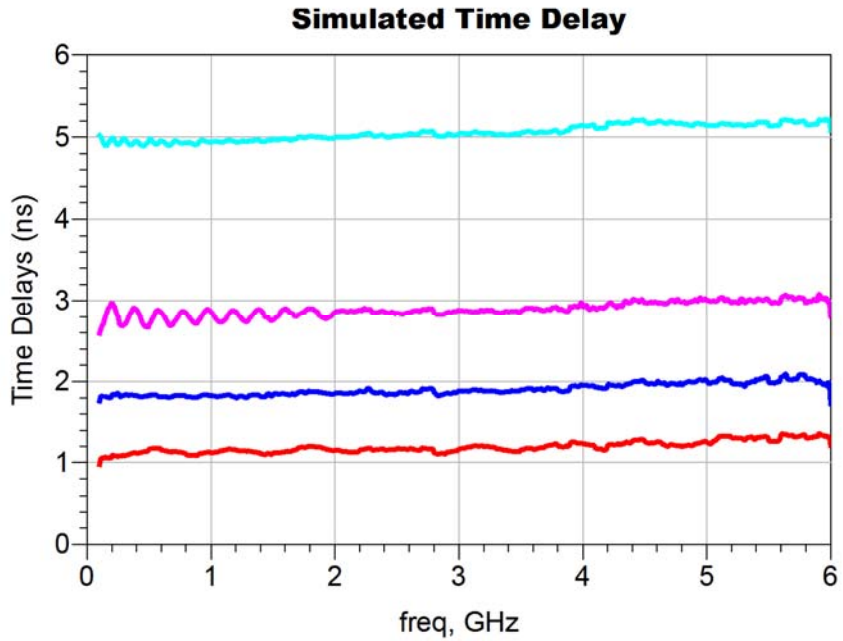
Amplifier

Switch

Attenuator

Results from Simulation for Completed TTD





Conclusions

- Demonstrate a TTD in HyperBGA board
- Embedded delayed lines to reduce the module size
- Demonstrate simulation of amplitude-compensated TTD. Complete layout.
- The full TTD module will be built soon in the near future
- We will perform test and evaluation

Ordering Information

Model Name	Ordering Part Number	Evaluation Board Part Number
SKY65014-70LF Low Noise Amplifier	SKY65014-70LF	SK40753

DATA SHEET

SKY13286-359LF: 0.1-6.0 GHz High Isolation SPDT Absorptive Switch

Applications

- GSM, PCS, WCDMA base stations
- 2.4 and 5.8 GHz ISM devices
- Wireless local loops

Features

- Single, positive voltage control: 0 to 3 and 0 to 5 V
- High isolation 64 dB at 1 GHz and 2 GHz
- Integrated silicon CMOS driver
- Absorptive
- Small, QFN (16-pin, 4 x 4 mm) Pb-free package (MSL1, 260 °C per JEDEC J-STD-020)

Skyworks Pb-free products are compliant with all applicable legislation. For additional information, refer to *Skyworks Definition of Lead (Pb)-Free*, document number SQ04-0073.

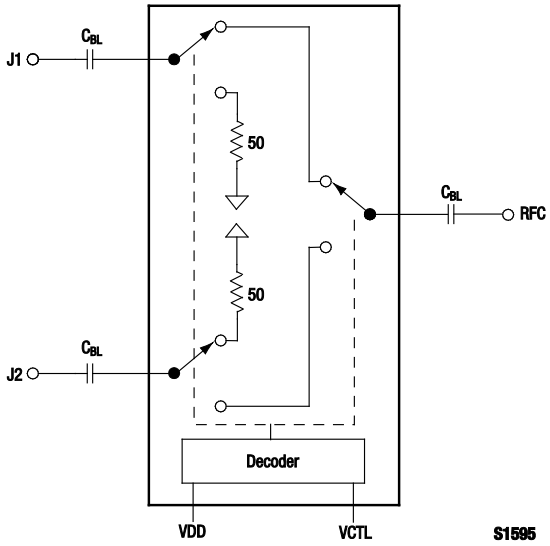


Figure 1. SKY13286-359LF Block Diagram

Description

The SKY13286-359LF is a GaAs pHEMT FET high-isolation, absorptive switch. The device is an ideal component for base station applications in which synthesizer isolation is critical.

The device is provided in a 4 x 4 mm, 16-pin Quad Flat No-Lead (QFN) package. A functional block diagram is shown in Figure 1. The pin configuration and package are shown in Figure 2. Signal pin assignments and functional pin descriptions are provided in Table 1.

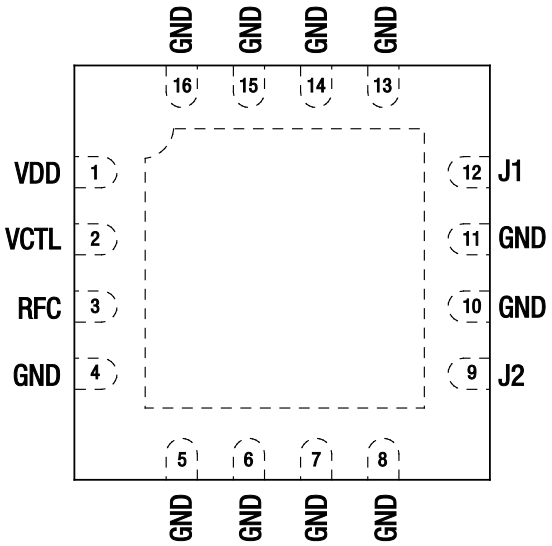


Figure 2. SKY13286-359LF Pinout – 16-Pin QFN (Top View)

Table 1. SKY13286-359LF Signal Descriptions

Pin #	Name	Description	Pin #	Name	Description
1	VDD	DC power supply	9	J2	RF output 2
2	VCTL	DC switch control pin. Switches insertion loss state from RFC to J1 or J2 (see Table 5).	10	GND	Ground
3	RFC	RF input	11	GND	Ground
4	GND	Ground	12	J1	RF output 1
5	GND	Ground	13	GND	Ground
6	GND	Ground	14	GND	Ground
7	GND	Ground	15	GND	Ground
8	GND	Ground	16	GND	Ground

Electrical and Mechanical Specifications

The absolute maximum ratings of the SKY13286-359LF are provided in Table 2. Recommended operating conditions are specified in Table 3 and electrical specifications are provided in Table 4.

Typical performance characteristics of the SKY13286-359LF are illustrated in Figures 3 through 9.

The state of the SKY13286-359LF is determined by the logic provided in Table 5.

Table 2. SKY13286-359LF Absolute Maximum Ratings

Parameter	Symbol	Minimum	Typical	Maximum	Units
Supply voltage	VDD	2.7		5.5	V
RF input power @ >500 MHz	V_I		1		W
Operating temperature	T_{OP}	–40		+95	°C
Storage temperature	T_{STG}	–65		+150	°C

Note: Exposure to maximum rating conditions for extended periods may reduce device reliability. There is no damage to device with only one parameter set at the limit and all other parameters set at or below their nominal value. Exceeding any of the limits listed here may result in permanent damage to the device.

***CAUTION**: Although this device is designed to be as robust as possible, Electrostatic Discharge (ESD) can damage this device. This device must be protected at all times from ESD. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD precautions should be used at all times.*

Table 3. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
Switching characteristics:						
Rise, fall		10/90% or 90/10% RF		30		ns
On/off		50% control to 90/10% RF		50		ns
Video feedthrough		T_{RISE} = 3 ns, measurement bandwidth = 500 MHz		25		mV
Input power for 1 dB compression	P_{INPUT}	VDD = 3V, 0.7-2.0 GHz		+23		dBm
		VDD = 5 V, 0.7-2.0 GHz	+26	+30		dBm
2nd harmonic	2fo	f_O = 2400 MHz, P_{IN} = –15 dBm		–80		dBm
3rd Order Intercept Point	IP3	For 2-tone input power, +8 dBm/tone, 1 MHz spacing:				
		VDD = 3.3 V, 0.7-1.0 GHz		+49		dBm
		VDD = 5.0 V, 0.7-1.0 GHz	+45	+47		dBm
		VDD = 3.3 V, 1.0-2.0 GHz		+43		dBm
		VDD = 5.0 V, 1.0-2.0 GHz	+45	+46		dBm
Control voltage (Note 1):						
Low with V_{DD} = 5 V	V_{CTL_LOW}		0		0.5	V
High with V_{DD} = 5 V	V_{CTL_HIGH}		2.7		VDD	V
Low with V_{DD} = 3.3 V	V_{CTL_LOW}		0		0.5	V
High with V_{DD} = 3.3 V	V_{CTL_HIGH}		2.5		3.3	V
Supply current		VDD = 5 V			100	µA
Control current		VCTL = low or high		5		µA
Supply voltage			2.7		5.0	V

Note 1: V_{DD} must be applied before a V_{CTL} high signal. A latch-up condition may occur if a logic high signal is applied before the V_{DD} voltage. Control voltages switch the V_{DD} voltage to the GaAs switch.

Table 4. SKY13286-359LF Electrical Specifications (Note 1)
(VCTL = 0 V/3 V, VDD = 5 V, T_{OP} = +25 °C, P_{INPUT} = 0 dBm, Characteristic Impedance [Z_0] = 50 Ω, Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
CW insertion loss	IL	0.1 to 2.0 GHz 2.0 to 3.0 GHz 3.0 to 4.0 GHz 4.0 to 6.0 GHz		0.8 0.8 1.0 1.5	1.10 1.25 1.35 1.80	dB dB dB dB
Isolation	Iso	0.1 to 2.0 GHz 2.0 to 3.0 GHz 3.0 to 4.0 GHz 4.0 to 6.0 GHz	60 58 55 40	62 62 58 42		dB dB dB dB
Return loss (insertion loss state) (Note 2)	RL	0.1 to 2.0 GHz 2.0 to 3.0 GHz 3.0 to 4.0 GHz 4.0 to 6.0 GHz	10 15 13 10	22 22 18 12		dB dB dB dB
Return loss (isolation state) (Note 2)	RL	0.1 to 2.0 GHz 2.0 to 3.0 GHz 3.0 to 4.0 GHz 4.0 to 6.0 GHz	10 12 12 11	12 15 15 13		dB dB dB dB
Insertion loss settling time	ΔIL	Insertion loss in db measured @ 1 μs (referenced to a rising 10% RF level on J1 & J2) minus the CW insertion loss in dB. Freq = 2 GHz, T_{OP} = +25 °C, V_{CTL} = 5 V, pulse width = 1.15 ms, 50% duty cycle.			0.40	dB

Note 1: Performance is guaranteed only under the conditions listed in this Table.

Note 2: Lower frequency return loss is dependent on DC blocks.

Typical Performance Characteristics

(VCTL = 0 V/3 V, VDD = 5 V, T_{OP} = +25 °C, P_{INPUT} = 0 dBm, Characteristic Impedance [Z_0] = 50 Ω, Unless Otherwise Noted)

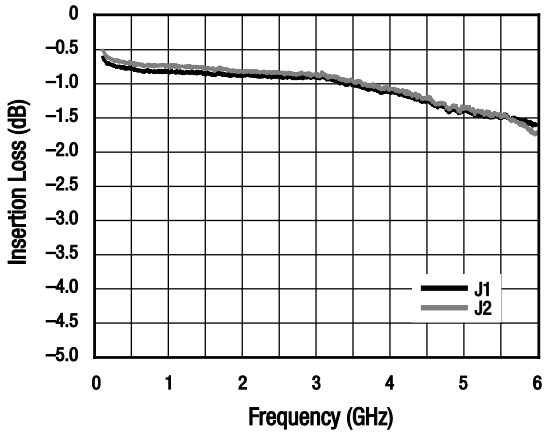


Figure 3. Insertion Loss vs Frequency

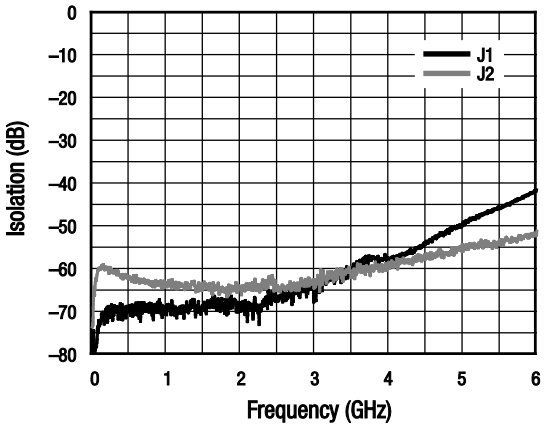


Figure 4. Isolation v s Frequency

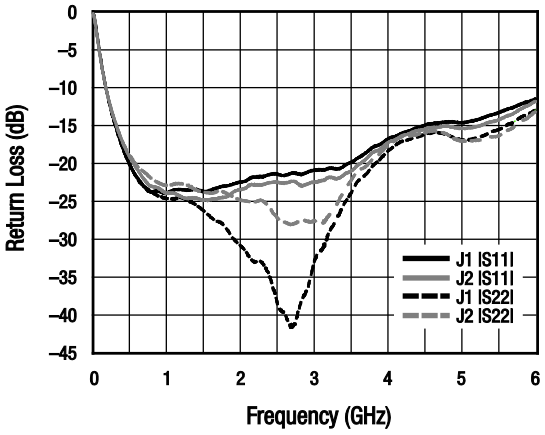


Figure 5. Return Loss vs Frequency (Insertion Loss State)

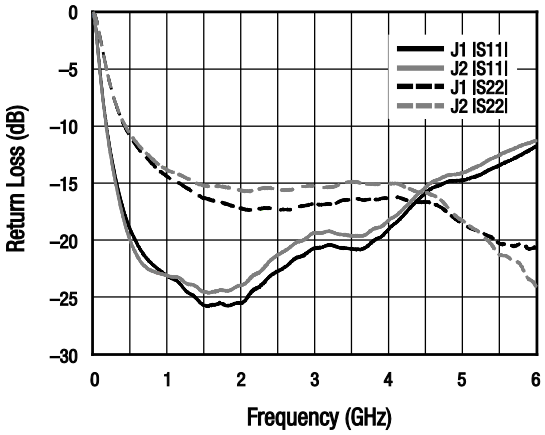


Figure 6. Return Loss vs Frequency (Isolation State)

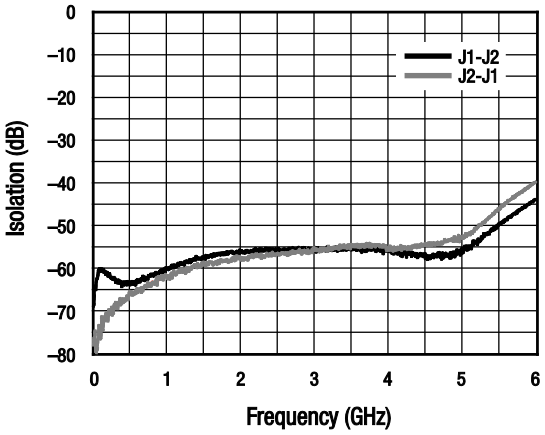


Figure 7. Output to Output Isolation

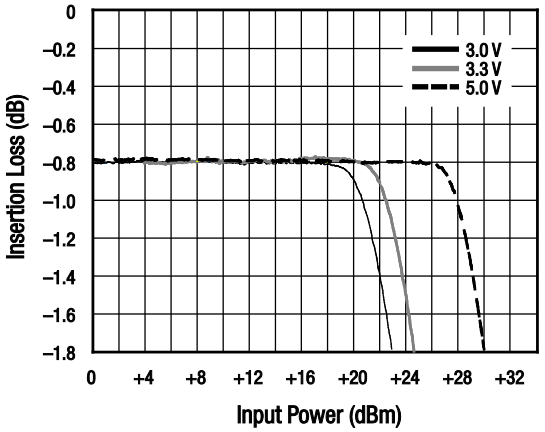


Figure 8. Insertion Loss vs Input Power Over Voltage

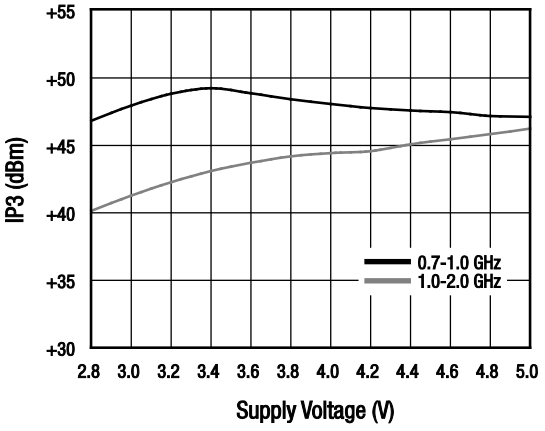


Figure 9. IP3 vs VDD Supply Voltage

Table 5. SKY13286-359LF Truth Table

VCTL	RFC to J1	RFC to J2
0	Insertion loss	Isolation
1	Isolation	Insertion loss

Evaluation Board Description

The SKY13286-359LF Evaluation Board is used to test the performance of the SKY13286-359LF SPDT absorptive switch. An assembly drawing for the Evaluation Board is shown in Figure 10.

Package Dimensions

The PCB layout footprint for the SKY13286-359LF is shown in Figure 11. Typical case markings are noted in Figure 12. Package dimensions for the 16-pin QFN are shown in Figure 13, and tape and reel dimensions are provided in Figure 14.

Package and Handling Information

Instructions on the shipping container label regarding exposure to moisture after the container seal is broken must be followed. Otherwise, problems related to moisture absorption may occur when the part is subjected to high temperature during solder assembly.

THE SKY13286-359LF is rated to Moisture Sensitivity Level 1 (MSL1) at 260 °C. It can be used for lead or lead-free soldering. For additional information, refer to the Skyworks Application Note, *Solder Reflow Information*, document number 200164.

Care must be taken when attaching this product, whether it is done manually or in a production solder reflow environment. Production quantities of this product are shipped in a standard tape and reel format.

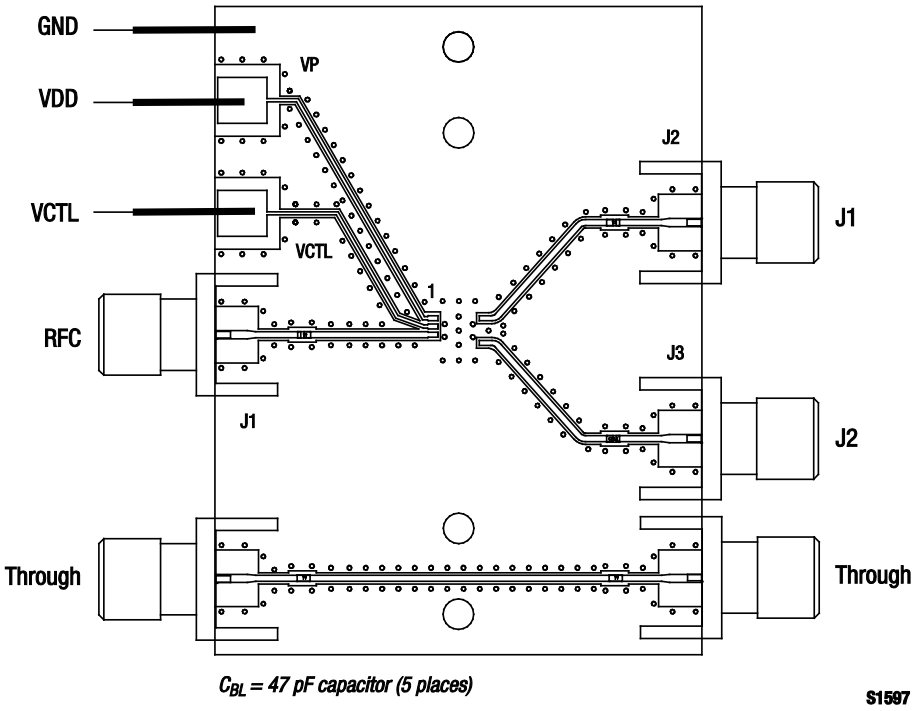


Figure 10. SKY13286-359LF Evaluation Board Assembly Diagram

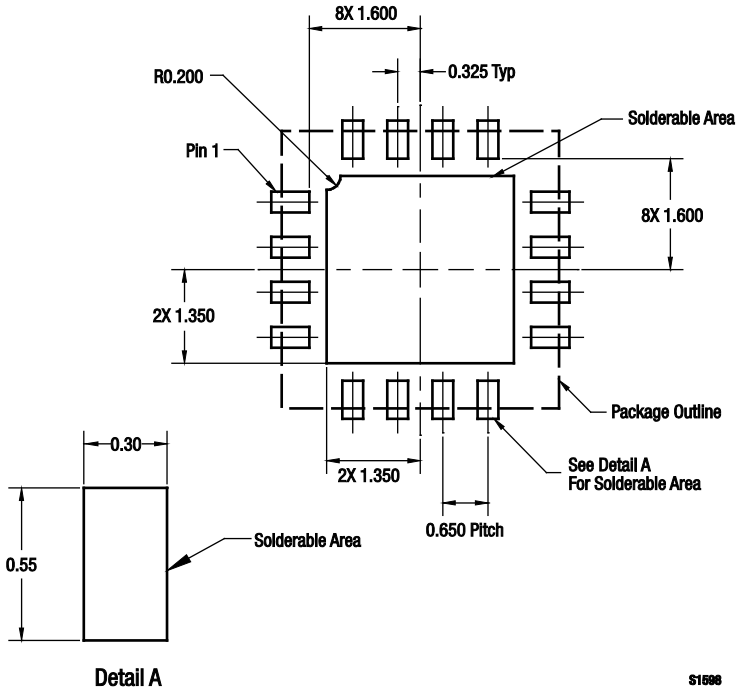


Figure 11. SKY13286-359LF PCB Layout Footprint

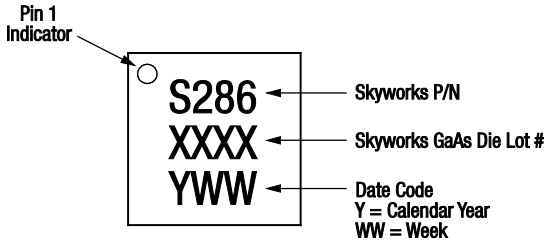


Figure 12. Typical Case Markings

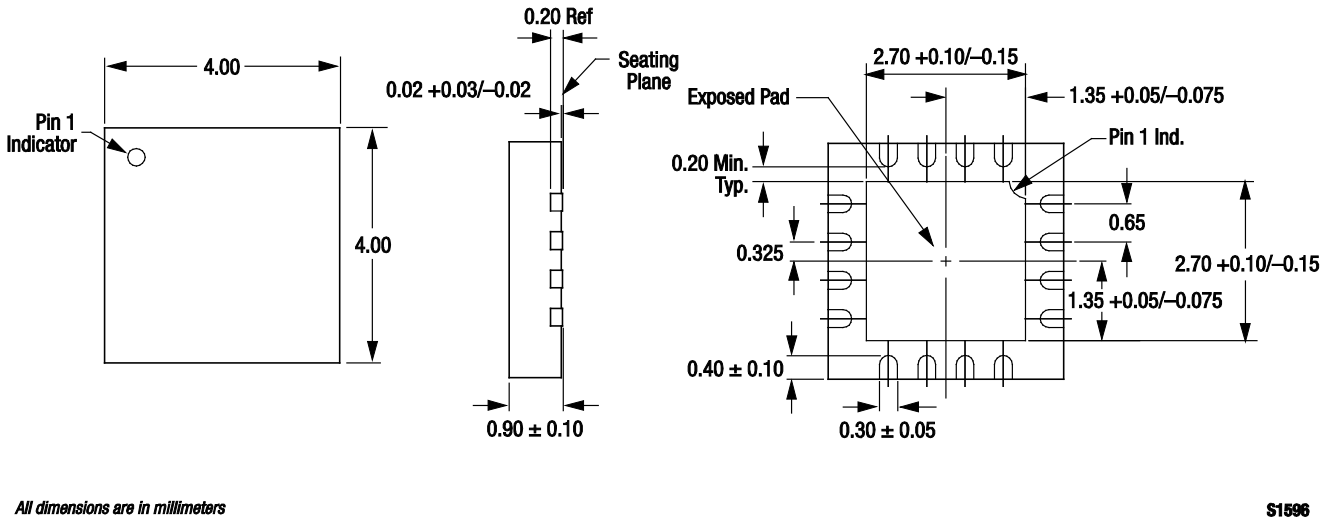


Figure 13. SKY13286-359LF 16-Pin QFN Package Dimensions

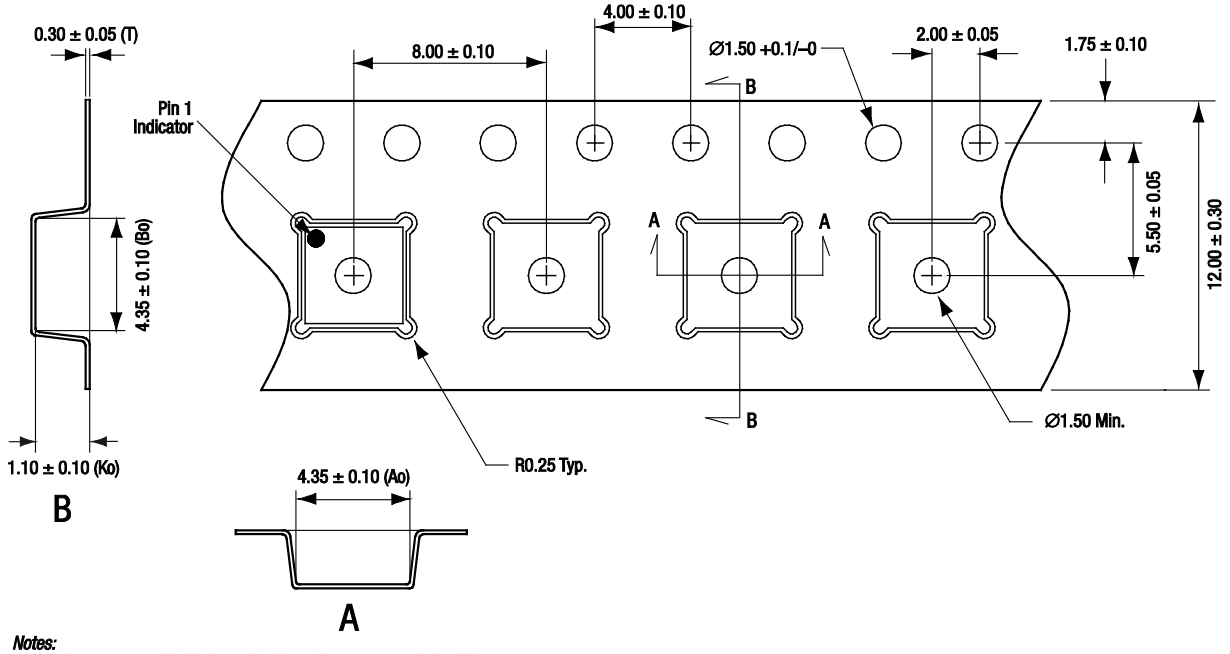


Figure 14. SKY13286-359LF Tape and Reel Dimensions

Ordering Information

Model Name	Manufacturing Part Number	Evaluation Board Part Number
SKY13286-359LF SPDT Absorptive Switch	SKY13286-359LF	SK39110, rev. 2

DATA SHEET

SKY12347-362LF: DC-3.0 GHz Six-Bit Digital Attenuator with Serial or Parallel Driver (0.5 dB LSB)

Applications

- Cellular, 3G/4G, WiMAX, and LTE Infrastructures

Features

- Broadband operation: DC to 3.0 GHz
- Attenuation: 31.5 dB with 0.5 dB LSB
- TTL/CMOS-compatible serial, parallel, or latched parallel control interface
- Single supply voltage: +3.3 or +5 V
- Small, QFN (24-pin, 4 x 4 mm) package (MSL1, 260 °C per JEDEC J-STD-020)

Skyworks Green™ products are compliant with all applicable legislation and are halogen-free. For additional information, refer to *Skyworks Definition of Green™*, document number SQ04-0074.

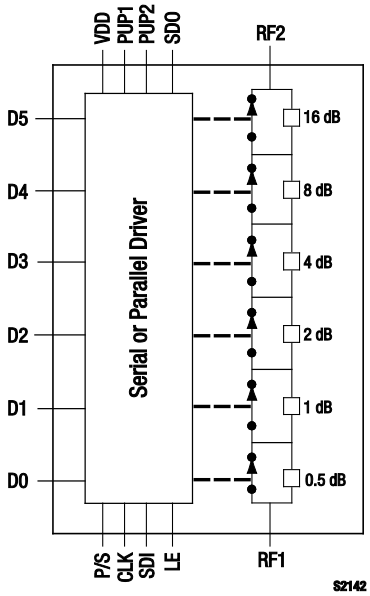


Figure 1. SKY12347-362LF Block Diagram

Description

The SKY12347-362LF is a GaAs pHEMT six-bit broadband digital attenuator with a 0.5 dB Least Significant Bit (LSB). A Transistor-to-Transistor Logic (TTL)/CMOS-compatible, dual-mode serial or parallel interface controller is integrated into the device.

The attenuator features low insertion loss, excellent attenuation accuracy, a 31.5 dB attenuation range, and high linearity performance. The SKY12347-362LF is an ideal choice for a wide variety of cellular 3G and 4G infrastructure applications.

Attenuation is controlled by a Serial Peripheral Interface (SPI). Depending on the SPI sequence applied to the SDI pin, the attenuation state between the RF1 and RF2 pins can vary between a low insertion loss state or up to 31.5 dB. The D0 through D5 DC control pins determine the attenuation state if parallel mode is enabled.

The device is provided in a 4 x 4 mm, 24-pin Quad Flat No-Lead (QFN) package. A functional block diagram is shown in Figure 1. The pin configuration and package are shown in Figure 2. Signal pin assignments and functional pin descriptions are provided in Table 1.

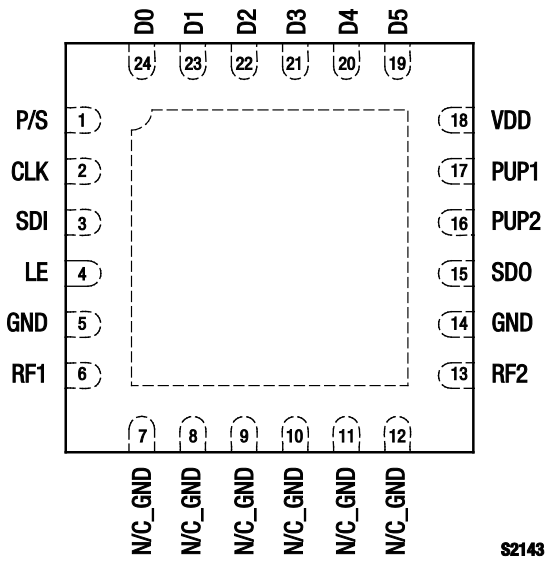


Figure 2. SKY12347-362LF Pinout – 24-Pin QFN
(Top View)

Table 1. SKY12347-362LF Signal Descriptions

Pin #	Name	Description	Pin #	Name	Description
1	P/S	Selects serial or parallel operation. Logic low enables parallel mode.	13	RF2	RF input/output to digital attenuator.
2	CLK	Serial clock input	14	GND	Ground
3	SDI	Serial data input	15	SDO	Serial data output
4	LE	On rising edge of pulse, shifts six most recent clocked-in bits to set attenuation state. In parallel mode, if latch enable is logic high, changes to pins 19 to 24 occur directly. If latch enable is logic low, the attenuator does not change states until the signal is raised.	16	PUP2	Sets device power-up attenuation state. See Table 7.
5	GND	Ground	17	PUP1	Sets device power-up attenuation state. See Table 7.
6	RF1	RF input/output to digital attenuator.	18	VDD	DC power supply
7	NC_GND	No connection. Can be grounded without affecting performance.	19	D5	TTL/CMOS DC control pin for parallel mode operation. D5 is MSB.
8	NC_GND	No connection. Can be grounded without affecting performance.	20	D4	TTL/CMOS DC control pin for parallel mode operation
9	NC_GND	No connection. Can be grounded without affecting performance.	21	D3	TTL/CMOS DC control pin for parallel mode operation
10	NC_GND	No connection. Can be grounded without affecting performance.	22	D2	TTL/CMOS DC control pin for parallel mode operation
11	NC_GND	No connection. Can be grounded without affecting performance.	23	D1	TTL/CMOS DC control pin for parallel mode operation
12	NC_GND	No connection. Can be grounded without affecting performance.	24	D0	TTL/CMOS DC control pin for parallel mode operation. D0 is LSB.

Functional Description

The SKY12347-362LF is a six bit digital attenuator comprised of a GaAs attenuator and a silicon CMOS driver. The attenuation setting is controlled by an SPI. Attenuation is set by a stream of data that is clocked into the shift registers of the silicon chip by the clock signal. To set the attenuation state, a latch signal is sent to the appropriate pin to send the correct bias voltages to the GaAs attenuator.

More than one attenuator can be cascaded together and the data may be passed through one device to the other using the SDO signal (pin 15). The DC bias voltage to the silicon CMOS chip is applied to pin 18 (VDD).

Power-Up/Power-Down Timing

Serial input data (SDI pin) is shifted into the register on the rising edge of the clock (CLK pin), Least Significant Bit (LSB) first. The attenuator changes states on the rising edge of the latch enable (LE pin) signal, according to the most recent six bits of shifted data accepted since the previous falling edge of the latch enable signal. The serial data output is the serial input data delayed by six clock cycles.

Refer to the timing diagram in Figure 3 and timing parameter specifications in Table 2. Table 3 shows the transition states based on the LE and CLK signals.

Power-up sequence is as follows:

0. Connect ground

1. Apply V_{DD}

2. Set all inputs (CLK, SDI, LE)

The power-down sequence is the reverse of above.

Figure 4 shows an example of how to set the attenuator to the 0.5 dB state. The progression of the bit states vs the clock signal is shown. The timing diagram shows that when the latch enable signal goes high, the voltages D0 to D5 set the attenuator to the 0.5 dB state.

Electrical and Mechanical Specifications

The absolute maximum ratings of the SKY12347-362LF are provided in Table 4. Electrical specifications are provided in Tables 5 and 6.

Typical performance characteristics of the SKY12347-362LF are illustrated in Figures 5 through 11.

The state of the SKY12347-362LF is determined by the logic provided in Table 7.

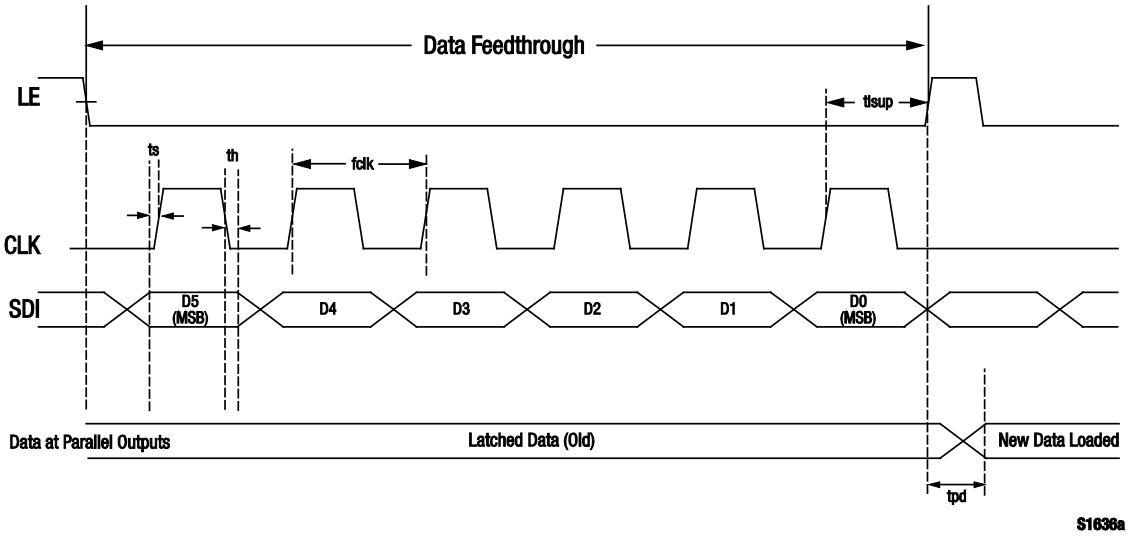


Figure 3. Power-Up/Power-Down Timing

Table 2. Power-Up/Power-Down Timing Parameters

Parameter	Symbol	V_{DD} = 5 V			V_{DD} = 3.3 V			Units
		Minimum	Typical	Maximum	Minimum	Typical	Maximum	
Serial input setup time	ts		5			5		ns
Hold time from serial input to shift clock	th		5			5		ns
Setup time from shift clock to latch enable	tlsup	40			100			ns
Propagation delay, latch enable to C0.5 through C8	tpd			30			70	ns
Setup time from reset to shift clock	–	20			50			ns
Clock frequency	f_{CLK}			30			10	MHz

Table 3. Transition State Logic

LE (Pin 4)	CLK (Pin 2)	Function
X	⟶	Shift register clocked
⟶	X	Contents of shift register transferred to digital attenuator

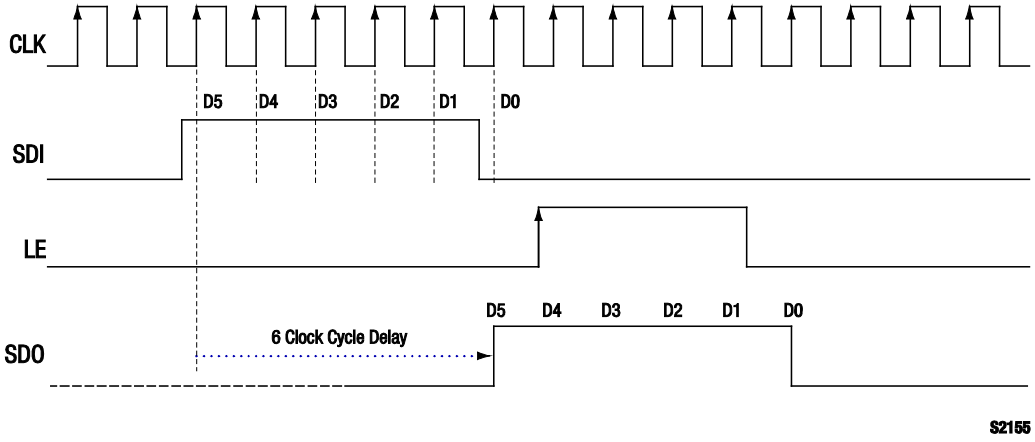


Figure 4. Example for Setting 0.5 dB State

Table 4. SKY12347-362LF Absolute Maximum Ratings

Parameter	Symbol	Minimum	Maximum	Units
Supply voltage	V_{DD}	3.3	6.0	V
Control voltage	V_{CTL}	0	V_{DD}	V
RF input power	P_{IN}		+30	dBm
Operating temperature	T_{OP}	–40	+85	°C
Storage temperature	T_{STG}	–40	+125	°C

Note: Exposure to maximum rating conditions for extended periods may reduce device reliability. There is no damage to device with only one parameter set at the limit and all other parameters set at or below their nominal value. Exceeding any of the limits listed here may result in permanent damage to the device.

***CAUTION**: Although this device is designed to be as robust as possible, Electrostatic Discharge (ESD) can damage this device. This device must be protected at all times from ESD. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD precautions should be used at all times.*

Table 5. SKY12347-362LF Electrical Specifications (Note 1) (1 of 2)
(V_{DD} = 5 V, V_{CTL} = 5 V, T_{OP} = +25 °C, P_{IN} = 0 dBm, Characteristic Impedance [Z_0] = 50 Ω, , Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
RF Specifications						
Insertion loss	IL	DC to 0.8 GHz 0.8 to 3.0 GHz		1.2 2.0	1.3 2.2	dB dB
Attenuation range		DC to 3.0 GHz	0.5		31.5	dB
Return loss	RL	DC to 3.0 GHz		15		dB
Attenuation accuracy		All attenuation states DC to 0.8 GHz 0.8 to 3.0 GHz		±(0.1 + 5% of attenuation setting max) ±(0.3 + 3% of attenuation setting max)		 dB dB
0.1 dB Input Compression Point	IP0.1dB	DC to 3.0 GHz		+30		dBm
3rd Order Input Intercept Point	IIP3	DC to 3.0 GHz, P_{IN} = +10 dBm/tone, ΔF = 1 MHz		+50		dBm
DC Specifications						
Control voltage: Low High	V_{CTL}		 0 3.0		 0.8 V_{DD}	 V V
Supply voltage	V_{DD}		3.3	5.0	5.5	V
Supply current	I_{DD}			100		µA

Table 5. SKY12347-362LF Electrical Specifications (Note 1) (2 of 2)
(V_{DD} = 5 V, V_{CTL} = 5 V, T_{OP} = +25 °C, P_{IN} = 0 dBm, Characteristic Impedance [Z_0] = 50 Ω, , Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
Switching Speed Specifications						
50% control to 90% attenuation		V_{DD} = 3.3 V, Bit = 3.3 V V_{DD} = 5.0 V, Bit = 3.3 V V_{DD} = 5.0 V, Bit = 5.0 V		91 48 47		ns ns ns
50% control to 10% attenuation		V_{DD} = 3.3 V, Bit = 3.3 V V_{DD} = 5.0 V, Bit = 3.3 V V_{DD} = 5.0 V, Bit = 5.0 V		19 28 28		ns ns ns
10% to 90% attenuation		V_{DD} = 3.3 V, Bit = 3.3 V V_{DD} = 5.0 V, Bit = 3.3 V V_{DD} = 5.0 V, Bit = 5.0 V		47 24 26		ns ns ns
90% to 10% attenuation		V_{DD} = 3.3 V, Bit = 3.3 V V_{DD} = 5.0 V, Bit = 3.3 V V_{DD} = 5.0 V, Bit = 5.0 V		35 18 18		ns ns ns

Note 1: Performance is guaranteed only under the conditions listed in this Table.

Typical Performance Characteristics

(V_{DD} = 5 V, V_{CTL} = 5 V, T_{OP} = +25 °C, P_{IN} = 0 dBm, Characteristic Impedance [Z_0] = 50 Ω, , Unless Otherwise Noted)

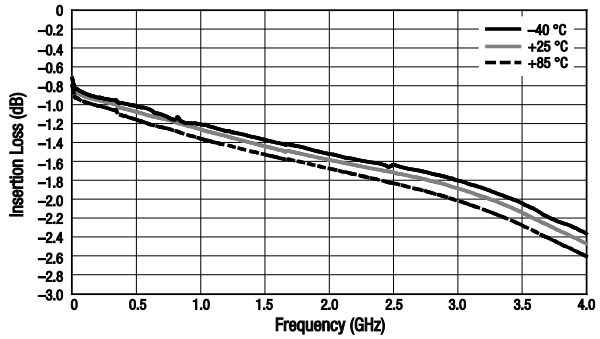


Figure 5. Insertion Loss vs Frequency

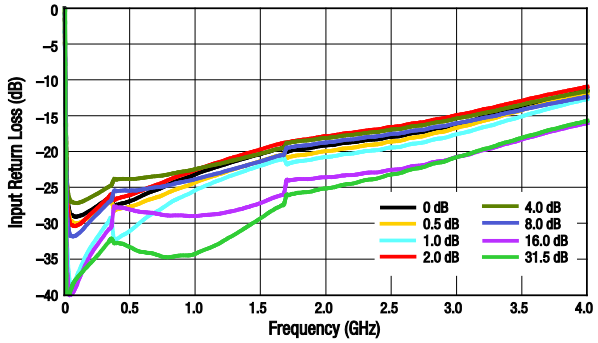


Figure 6. Input Return Loss vs Frequency

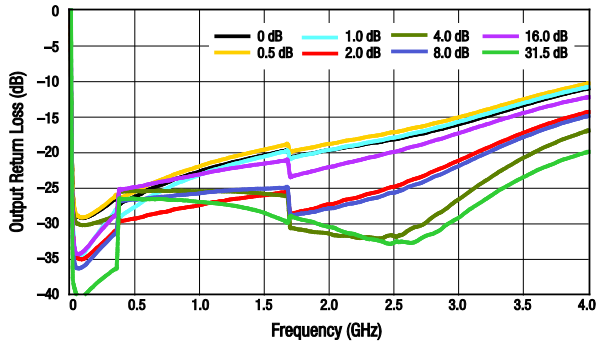


Figure 7. Output Return Loss vs Frequency

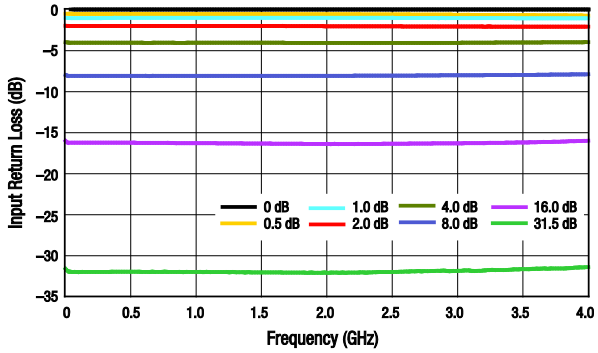


Figure 8. Normalized Attenuation vs Frequency

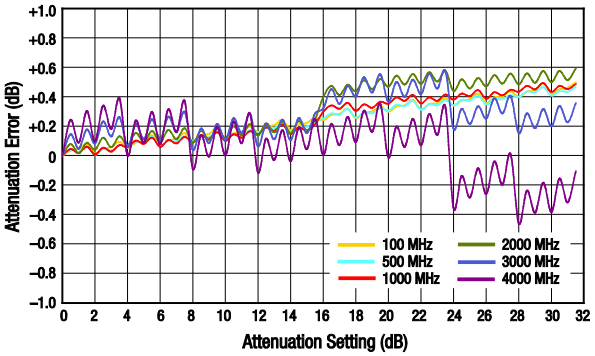


Figure 9. Attenuation Error vs Attenuation Setting

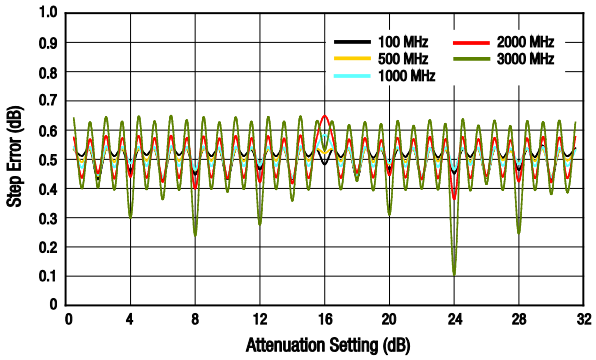


Figure 10. Step Error vs Attenuation Setting

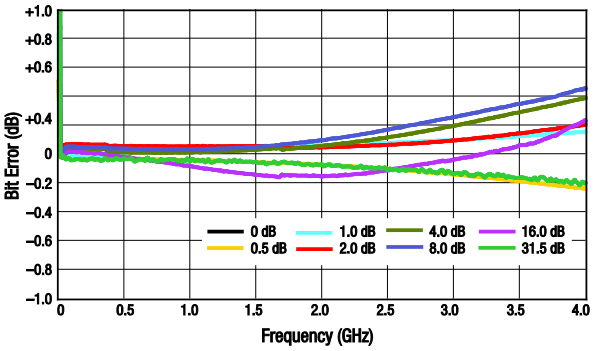


Figure 11. Major State Bit Error vs Frequency

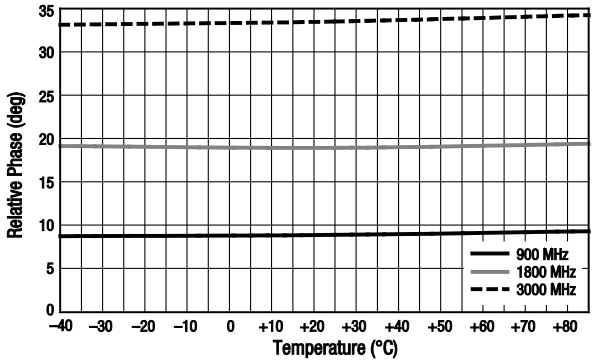


Figure 12. 31.5 dB State Relative Phase vs Temperature

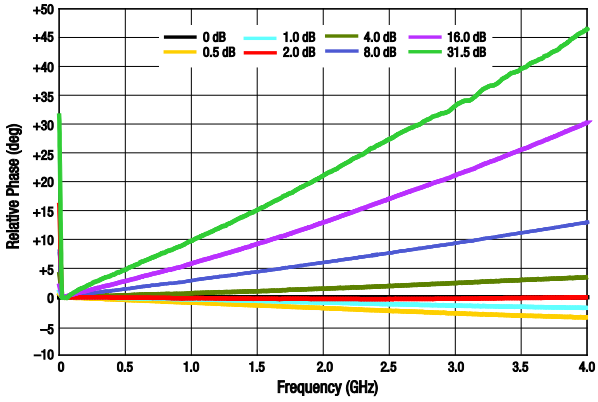


Figure 13. Relative Phase vs Frequency

Table 6. SKY12347-362LF Parallel Mode Truth Table

RF1/RF2 (Pins 6 & 13) Attenuation	D5 (Pin 19)	D4 (Pin 20)	D3 (Pin 21)	D2 (Pin 22)	D1 (Pin 23)	D0 (Pin 24)
Insertion loss	1	1	1	1	1	1
0.5 dB	1	1	1	1	1	0
1.0 dB	1	1	1	1	0	1
2.0 dB	1	1	1	0	1	1
4.0 dB	1	1	0	1	1	1
8.0 dB	1	0	1	1	1	1
16 dB	0	1	1	1	1	1
31.5 dB	0	0	0	0	0	0

Note: "1" = high control voltage: +3.0 to V_{DD}.
"0" = low control voltage: 0 to +0.8 V.

Table 7. SKY12347-362LF Power-Up Truth Table

Initial Attenuation State	LE (Pin 4)	PUP1 (Pin 17)	PUP2 (Pin 16)
31.5 dB	0	0	0
24.0 dB	0	1	0
16.0 dB	0	0	1
Insertion Loss	0	1	1
State is determined by signal logic at pins D0 to D5. See Table 6.	1	X	X

Note: "1" = Logic high
"0" = Logic low
"X" = don't care

Evaluation Board Description

The SKY12347-362LF Evaluation Board is used to test the performance of the SKY12347-362LF digital attenuator. An assembly drawing for the Evaluation Board is shown in Figure 14 and an Evaluation Board schematic diagram is shown in Figure 15.

Package Dimensions

The PCB layout footprint for the SKY12347-362LF is shown in Figure 16. Typical case markings are noted in Figure 17. Package dimensions for the 24-pin QFN are shown in Figure 18, and tape and reel dimensions are provided in Figure 19.

Package and Handling Information

Instructions on the shipping container label regarding exposure to moisture after the container seal is broken must be followed. Otherwise, problems related to moisture absorption may occur when the part is subjected to high temperature during solder assembly.

THE SKY12347-362LF is rated to Moisture Sensitivity Level 1 (MSL1) at 260 °C. It can be used for lead or lead-free soldering. For additional information, refer to the Skyworks Application Note, *Solder Reflow Information*, document number 200164.

Care must be taken when attaching this product, whether it is done manually or in a production solder reflow environment. Production quantities of this product are shipped in a standard tape and reel format.

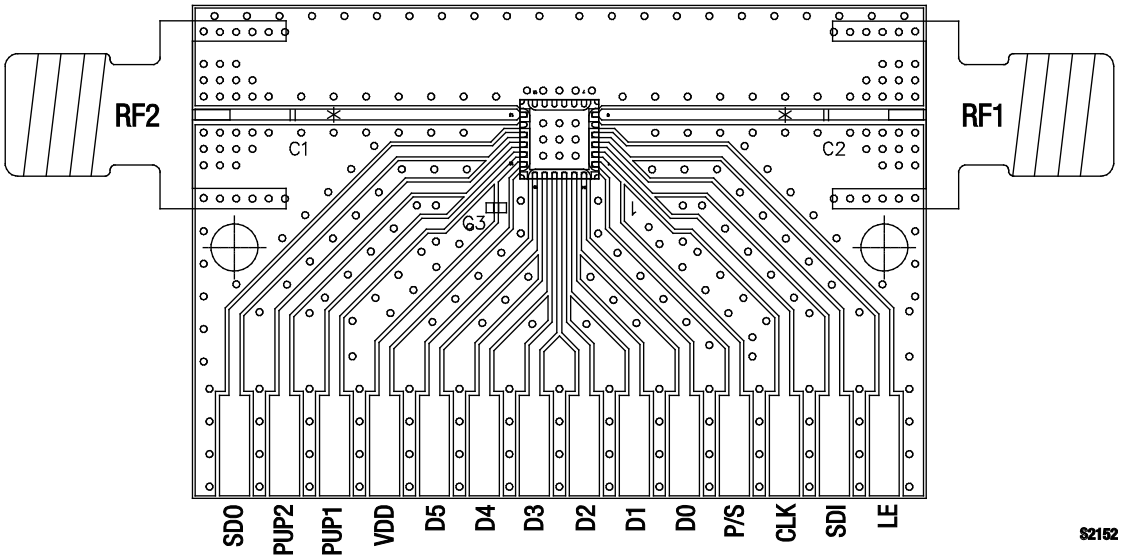


Figure 14. SKY12347-362LF Evaluation Board Assembly Diagram

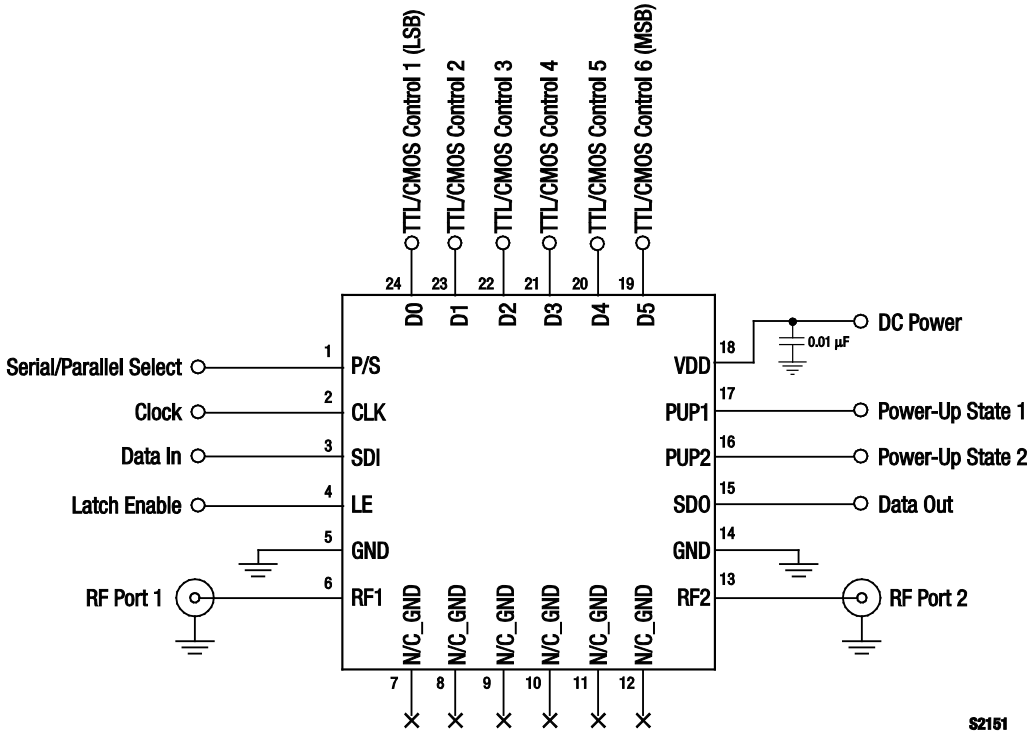


Figure 15. SKY12347-362LF Evaluation Board Schematic Diagram

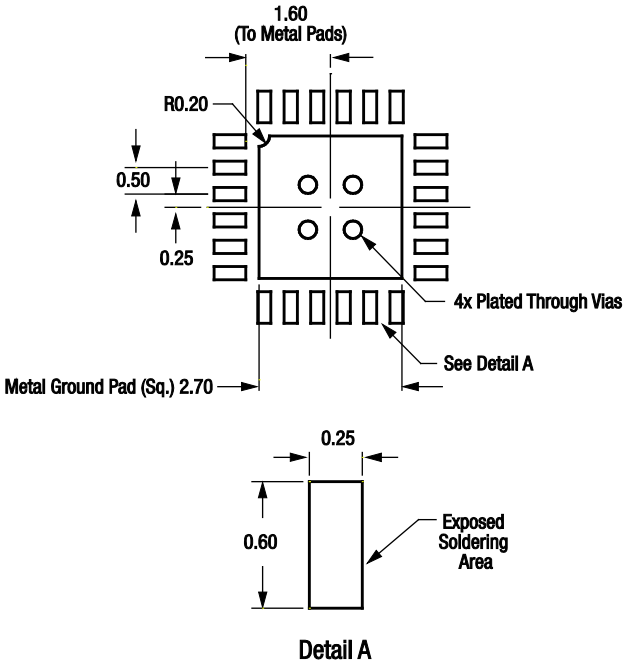


Figure 16. SKY12347-362LF PCB Layout Footprint

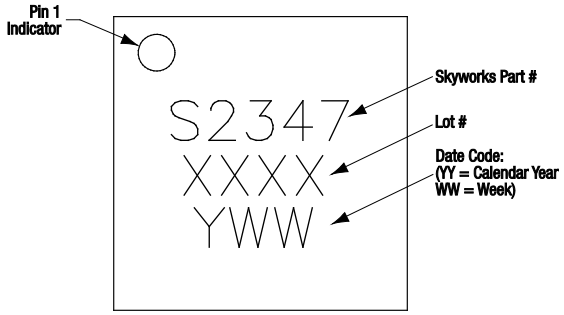


Figure 17. Typical Part Markings

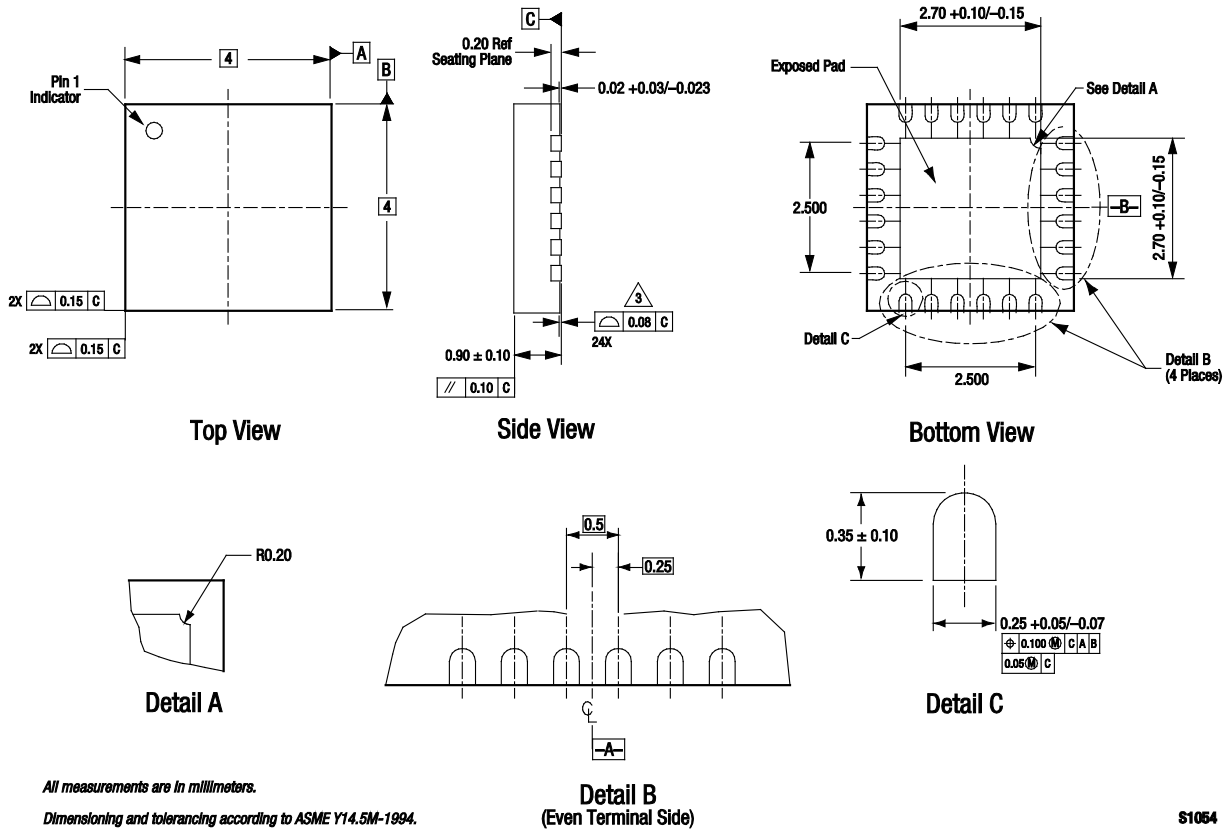


Figure 18. SKY12347-362LF 24-Pin QFN Package Dimensions

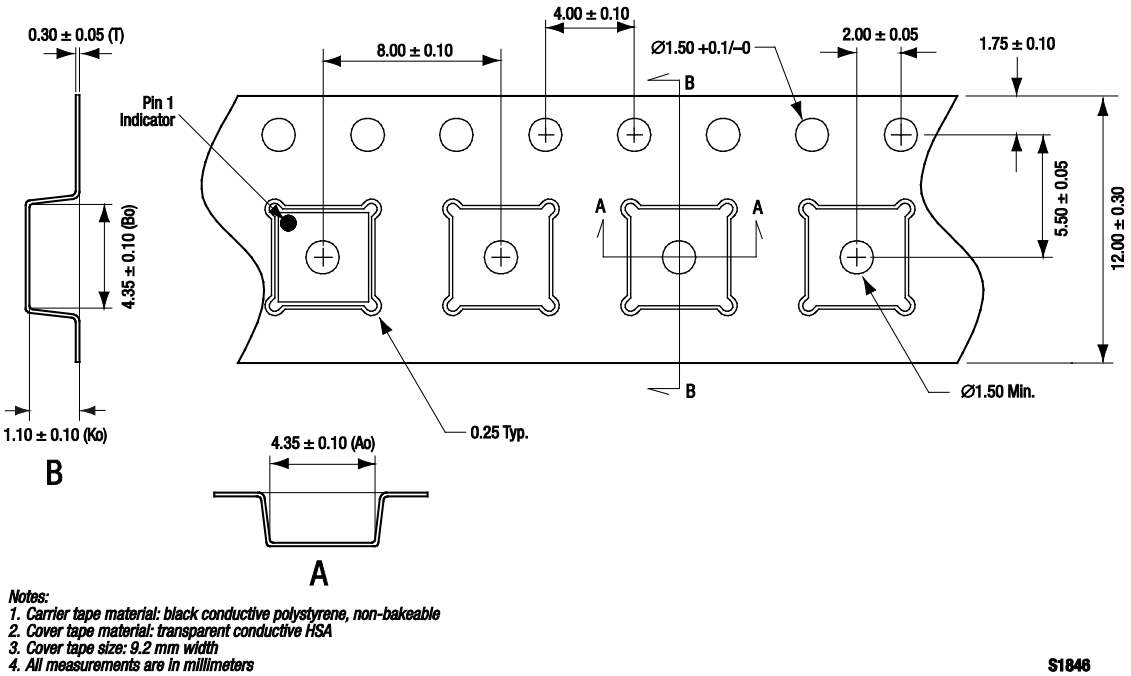


Figure 19. SKY12347-362LF Tape and Reel Dimensions

Ordering Information

Model Name	Manufacturing Part Number	Evaluation Board Part Numbers
SKY12347-362LF Digital Attenuator	SKY12347-362LF	SKY12347-362LF-EVB